CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CMX990

GMSK Packet Data Modem and RF Transceiver

D/990/1 April 2004

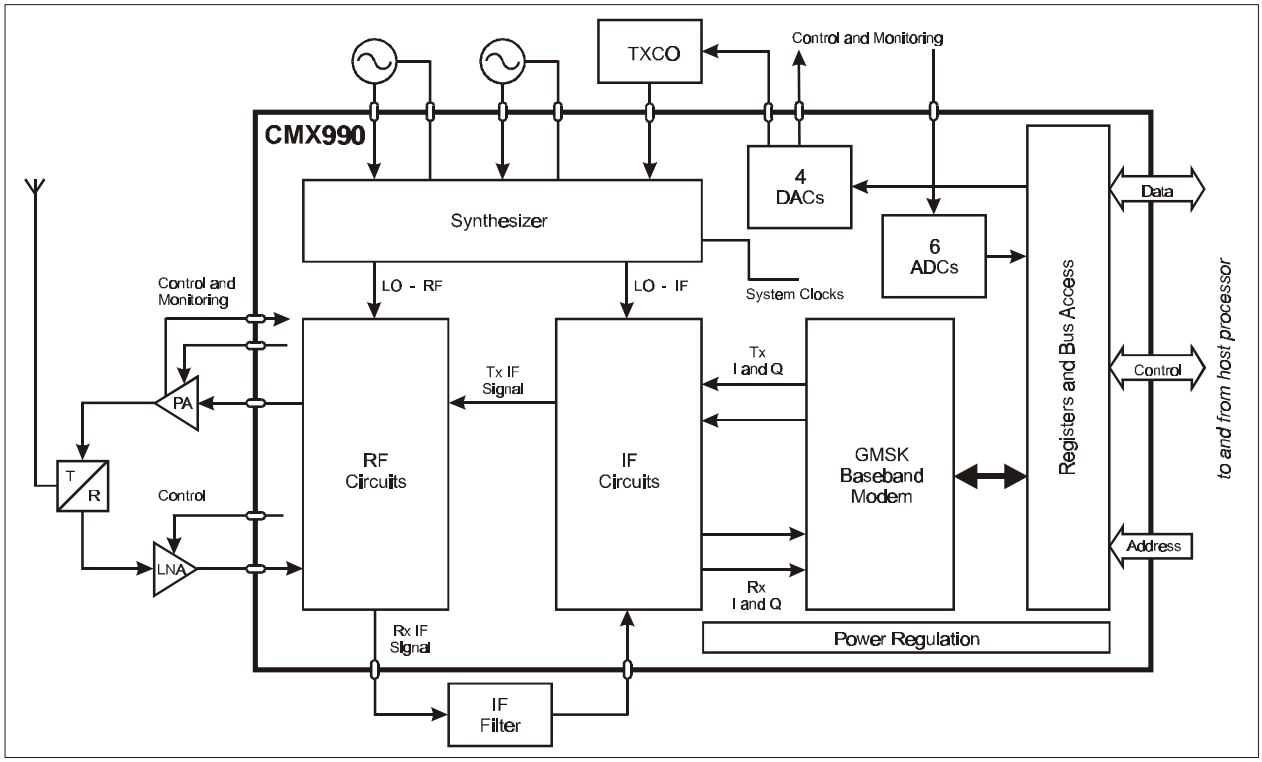
Advance Information

Features

- Single Chip RF Transceiver and GMSK Modem
- IF, RF, Control and Synthesizer Stages
- Selectable B_t = 0.3 or 0.5
- Full Mobitex Compatibility
- Packet and Freeformat (Raw) Data
- Versatile Data Rates: 4kbps to 16kbps
- Simple Parallel Interfacing
- Low-Power, Low Profile, Low-Cost BOM
- Flexible System Clocks

Applications

- Narrowband Data Over Radio
- Mobitex Data Terminals
- 400MHz to 1GHz Radio Data Systems
- Radio Modems
- Wireless Telemetry
- SCADA Terminals
- Suitable for EN 300 113 and FCC CFR 47 Part 90 Applications



1. Brief Description

A single-chip GMSK packet-data modem and RF transceiver, the CMX990 provides the majority of circuits and functions, including host µC interfaces, to implement a full-feature 'wireless modem' subsystem. The CMX990 can operate in RF ranges of 400MHz to 1GHz at data rates of 4 to 16 kbps and is fully Mobitex compatible.

With a minimum of external components and circuits, this half-duplex device provides on-chip: a flexible, formattable GMSK packet and freeformat modem, a dual operation synthesiser fed from an external source, IF and RF stages for both Rx and Tx modes, and auxiliary ADCs and DACs for system control and monitoring.

This versatile GMSK modem is programmable to both packet and freeformat data operations via an efficient task-oriented Rx and Tx format and command structure, which is combined with data scrambling, interleaving and FEC and CRC capabilities. Rx data acquisition, extraction and tracking abilities, allied with Rx data quality feedback, allow the CMX990 to operate seamlessly in varying signal environments.

IF and RF functions in the Tx path handle all the required signal mixing and up-conversion to produce the FM modulation for the final external PA circuitry. In the Rx path these circuits provide initial selectivity and rejection characteristics and mix down the inputs to provide baseband signals for the modem.

Comprehensive internal and external system control and monitoring is provided by the 8-bit host interface registers and the on-chip ADCs and DACs. Requiring a power supply input in the range 3.0 to 3.6 Volts, the CMX990 can be used in wireless products designed to comply with such standards as EN 300 113 and FCC CFR 47 Part 90. Operating over a temperature range of -40°C to +85°C, the CMX990 consolidates the core radio modem functions to enable a new generation of small, narrow-band wireless data modems. The CMX990 comes in a 64-pin low profile VQFN package.

CONTENTS

It is always recommended that you check for the latest product datasheet version from the Datasheets page of the CML website: [www.cmlmicro.com].

Note: This product is in development: Changes and additions will be made to this specification. Items marked TBD or left blank will be included in later issues.

Information in this data sheet should not be relied upon for final product design.

2. Block Diagram

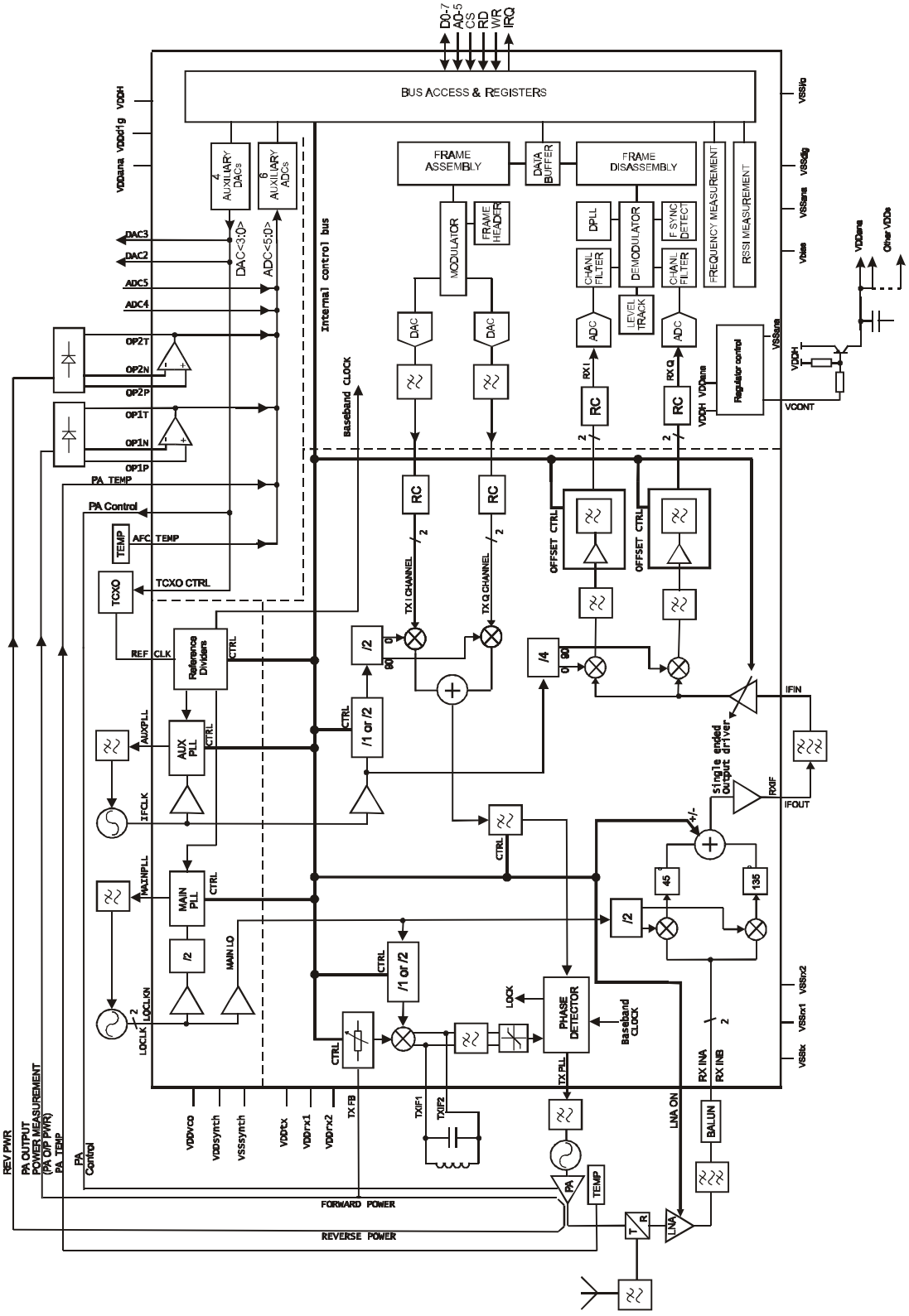


Figure 1 Block Diagram

3. Signal List

Package Q1	Signal		Description
Pin No.	**Name**	**Type**	
1	PA-CNTL	O/P	DAC0 output to control PA power.
2	TX FB	I/P	Tx feedback input signal.
3	TXIF2	BI	Offset loop filter connection.
5	TXIF1	BI	Offset loop filter connection.
7	TXPLL	O/P	Tx Phase Detector output.
8	RF IN A	I/P	RF input A for received signal.
9	RF IN B	I/P	RF input B for received signal.
11	IF OUT	O/P	Output to the external IF filter.
14	LNA ON	O/P	Digital output to turn on external LNA block.
16	IF IN	I/P	Input from the external IF filter.
43	DAC3	O/P	Spare D/A output.
44	DAC2	O/P	Spare D/A output.
45	ADC5	I/P	Spare A/D input.
46	ADC4	I/P	Spare A/D input.
47	OP2T	O/P	Uncommitted op-amp 2 output, internally connected to ADC3.
48	OP2N	I/P	Uncommitted op-amp 2 negative input.
49	OP2P	I/P	Uncommitted op-amp 2 positive input.
50	OP1T	O/P	Uncommitted op-amp 1 output, internally connected to ADC2.
51	OP1N	I/P	Uncommitted op-amp 1 negative input.
52	OP1P	I/P	Uncommitted op-amp 1 positive input.
53	REFCLK	I/P	Master clock input from external TCXO.
54	TCXO-CNTL	O/P	DAC1 output to control TCXO.
55	TCXO-TEMP	I/P	A/D input to measure TCXO temperature, internally connected to ADC1.
56	LOCLKN	I/P	Inverted input from the RF Oscillator circuit.
57	LOCLK	I/P	Input from the RF Oscillator circuit.
59	MAINPLL	O/P	Main PLL output, connect to external filter.
61	AUXPLL	O/P	Aux PLL output, connect to external filter.
63	IFCLK	I/P	Input from the IF Oscillator circuit.
64	PA-TEMP	I/P	A/D input to measure PA temperature, internally connected to ADC0.

Package Q1	Signal		Description
Pin No.	**Name**	**Type**	
17	A5	I/P	Register address select logic inputs.
18	A4	I/P	"
19	A3	I/P	"
20	A2	I/P	"
21	A1	I/P	"
22	A0	I/P	"
29	RDN	I/P	Read. An active low logic level input used to control the reading of data from the modem into the controlling µC.
30	WRN	I/P	Write. An active low logic level input used to control the writing of data into the modem from the controlling µC.
31	CSN	I/P	Chip Select. An active low logic level input used to enable a data read or write operation.
32	IRQN	O/P	A 'wire-ORable' output for connection to the host Interrupt Request input. This output has a low impedance pull down to V_{SS} when active and is high impedance when inactive. An external pullup resistor is required.
34	D7	BI	Tri-state µC interface data line.
35	D6	BI	"
36	D5	BI	"
37	D4	BI	"
38	D3	BI	"
39	D2	BI	"
40	D1	BI	"
41	D0	BI	"

Package Q1	Signal		Description
Pin No.	**Name**	**Type**	
4	V_{DD} Tx	Power	Power supply to Tx IF and RF circuits.
6	V_{SS} Tx	Power	Return for V_{DD} Tx, good decoupling required.
10	V_{DD} Rx1	Power	Power supply to Rx RF circuits.
12	V_{SS} Rx1	Power	Return for V_{DD} Rx1, good decoupling required.
13	V_{SS} Rx2	Power	Return for V_{DD} Rx2, good decoupling required.
15	V_{DD} Rx2	Power	Power supply to Rx IF circuits.
23	V_{DD} Dig	Power	Power supply to base band digital circuits.
24	V_{DD} Ana	Power	Power supply to aux ADC, DAC, OP1/2 circuits.
25	V_{BIAS}	O/P	Output of internal bias generator, decouple to V_{SS} Ana.
26	V_{SS} Ana	Power	Return for V_{DD} Ana, good decoupling required.
27	V_{SS} Dig	Power	Return for V_{DD} Dig, good decoupling required.
28	V_{SS} H	Power	Return for V_{DD} H, good decoupling required.
33	V_{DD} H	Power	Power supply to host interface and 2.5V regulator circuit.
42	V-CONT	O/P	Control signal for external regulating transistor.
58	V_{SS} Synth	Power	Return for V_{DD} Synth, good decoupling required.
60	V_{DD} VCO	Power	Power supply to the VCO charge pump, decouple to V_{SS} H.
62	V_{DD} Synth	Power	Power supply to synthesiser circuits.

Notes:
I/P = Input
O/P = Output
BI = Bidirectional
T/S = 3-state Output
NC = No Connection

4. External Components

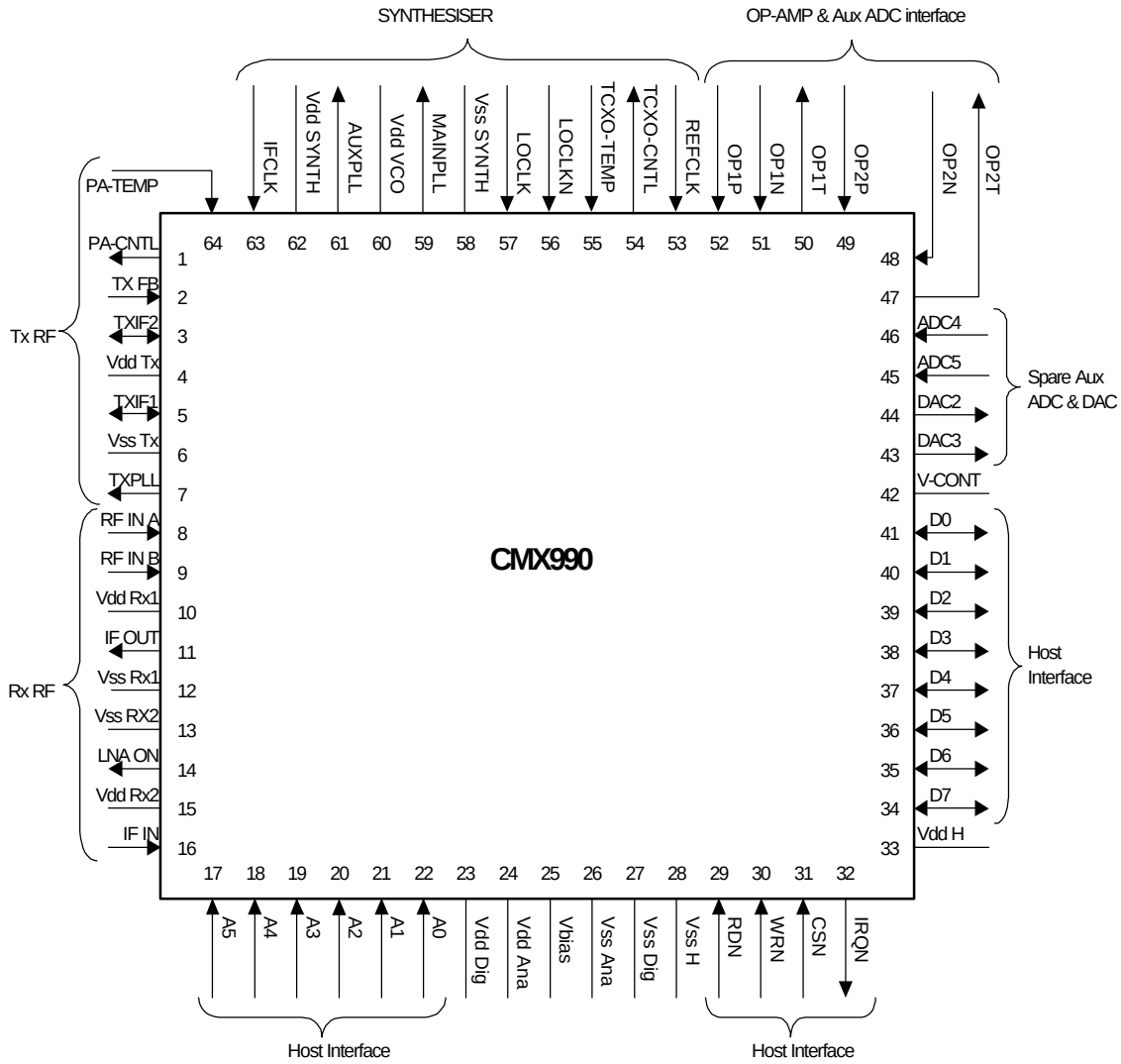


Figure 2 CMX990 Pin Overview

4.1 Processor Interface

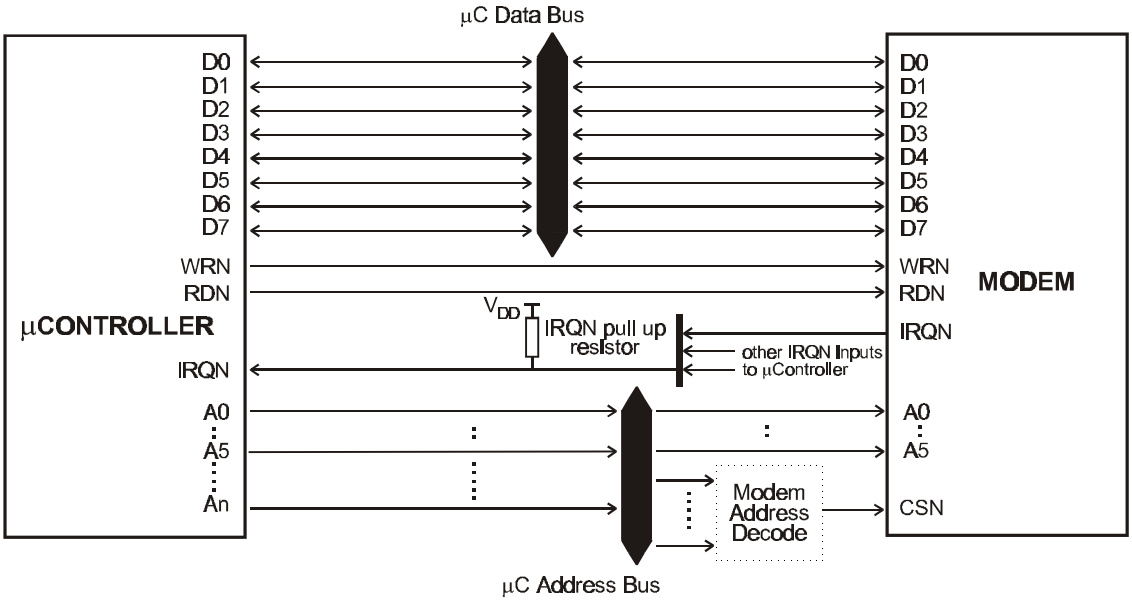


Figure 3 Recommended External Configuration - Processor Interface

4.2 Synthesiser and TCXO

The CMX990 synthesiser section provides two independent synthesisers. The PLLs implement a Type II loop with a phase / frequency phase detector providing an output of a charge pump current. Various types of loop filter can be used and should be optimised for VCO gain of a particular design. Figure 4 gives typical configuration and values.

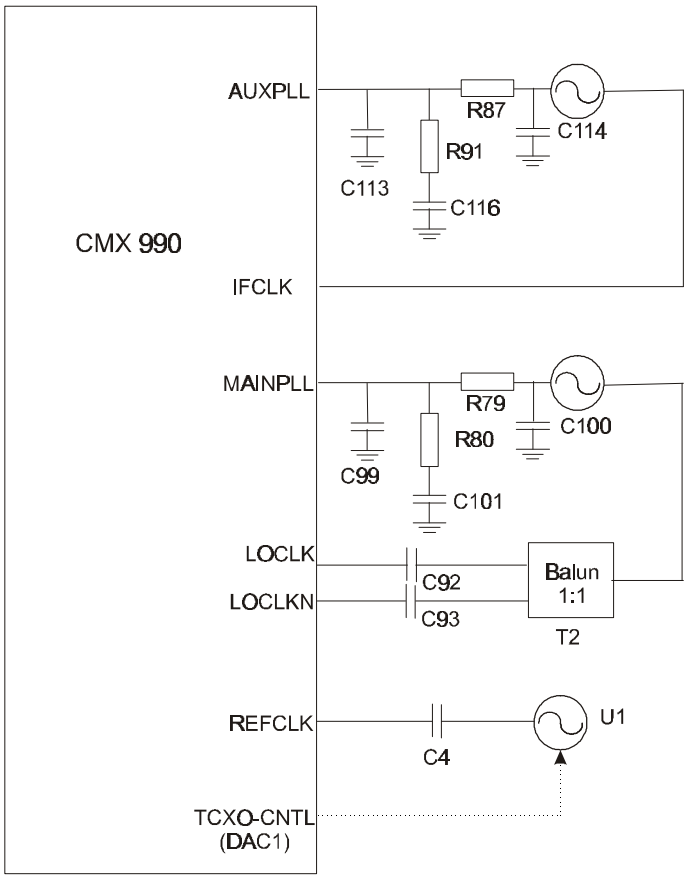


Figure 4 Recommended External Components - Synthesiser and TCXO

C4	1 nF	C114	1 nF
C92	1 nF	C116	150 nF
C93	1 nF	T2	TCM4-25
C99	27 nF	R79	2.7 kΩ
C100	27 nF	R80	1.2 kΩ
C101	680 nF	R87	39 kΩ
C113	1 nF	R91	1.5 kΩ
		U1	See notes

Notes:

1 Resistors ±2%, capacitors ±5% unless otherwise stated.
2 For optimum lock time / phase noise it is recommended C113 and C116 use a low piezo type such as PPS film; optimum performance is not guaranteed with X7R or Y5V types.
3 U1 Should be a VCTCXO or TCXO depending on application requirements. A typical device is the Golledge GTXO-81. The CMX990 has a high impedance input suitable for use with oscillators with clipped sine wave output. An external DC blocking capacitor (as shown, C4) is required.

4.3 Transmit

The CMX990 transmitter uses an offset phase-locked loop to accurately modulate RF signals. Details are contained in subsequent sections of this document. The components used around the CMX990 will depend on application requirements however a typical configuration is shown in Figure 5.

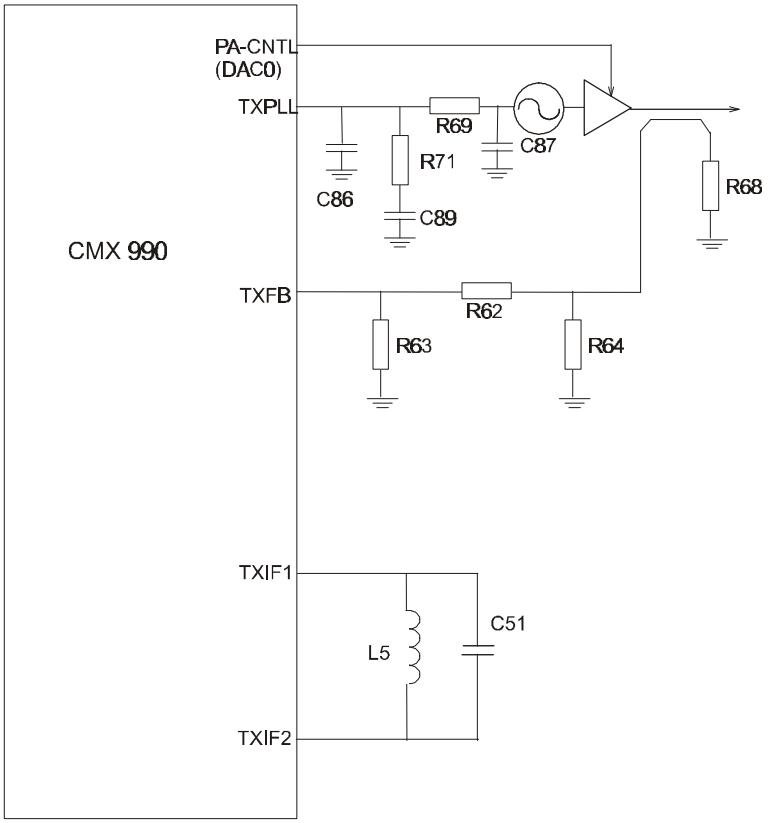


Figure 5 Recommended External Components - Transmit

C51	6.8 pF	R62	18 Ω
C86	15 nF	R63	270 Ω
C87	TBD nF	R64	270 Ω
C89	68 nF	R68	47 Ω
		R69	10 Ω
L5	270 nH	R71	36 Ω

Notes:

1 Resistors ±2%, capacitors ±5% unless otherwise stated.
2 The coupler may be a packaged type (e.g. 0869CP14A090) or printed on the PCB; alternatively a sample of the output can be obtained with a resistive or capacitive tap.
3 Tx loop filter components need to be optimised for selected VCO.
4 Components between TXIF1 and TXIF2 act as a resonant load to the mixer. They should be matched to the selected IF frequency whilst attenuating its odd harmonics. The Q of this filter can be controlled by changing the ratio of C51 to L5 whilst the centre frequency can be maintained by keeping the product of C51 and L5 a constant. A higher value of C51 will give a higher Q. The Q should not be so high as to prevent accommodation of the natural frequency range of the VCO. The values shown are approximate for an IF of 90MHz. Approximate values for an IF of 45MHz are 18pF and 560nH.

4.4 Receive

The receiver relies on external LNA, filtering and T/R switch; details can be found in the following sections. The 1st mixer in the CMX990 has a differential input. To ensure optimum performance a balun is required when driving from typical LNAs or filters. The balun may be a transformer type, which is implemented using LC networks. Suitable matching components around the balun, selected for the desired operating frequency, provide matching to 50Ω. Figure 6 shows a typical configuration for 800 - 840MHz operation.

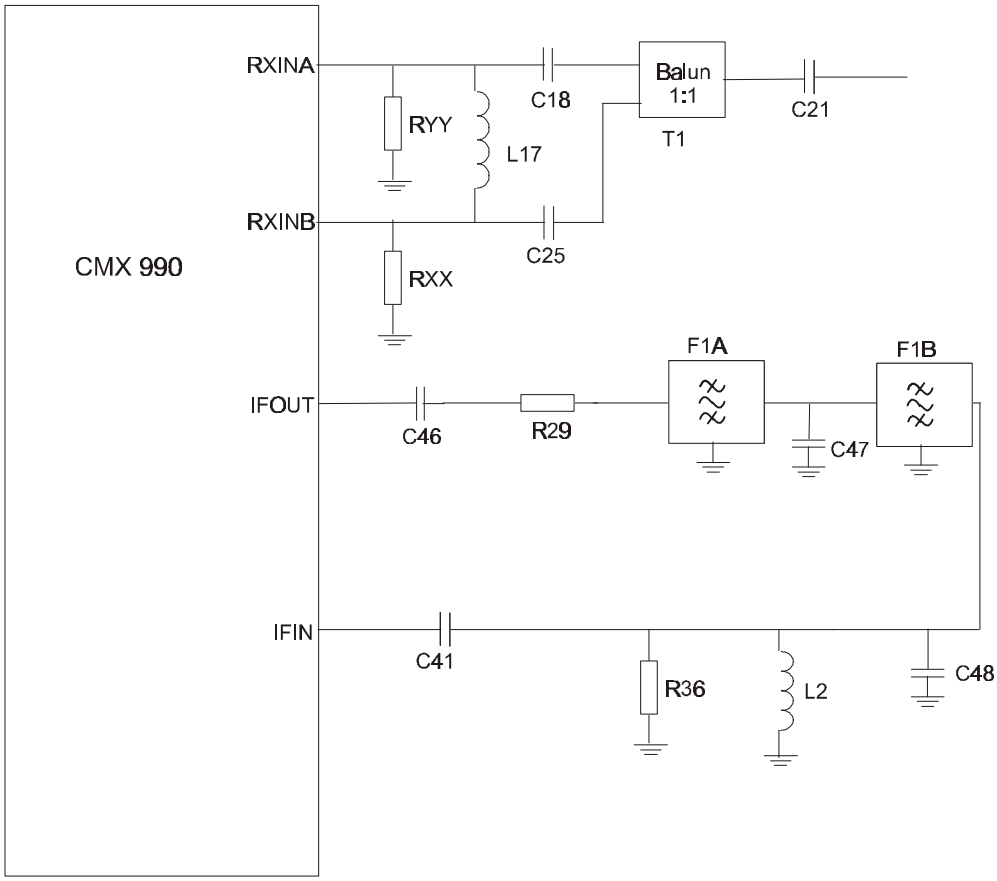


Figure 6 Recommended External Components - Receive

C18	5 pF	L2	1.2 µH
C21	1 nF	L17	15 nH
C25	5 pF	T1	2.7 kΩ
C41	1 nF	R29	330 Ω
C46	10 nF	R36	39 kΩ
C47	15 pF	RXX	100 Ω
C48	5.6 pF	RYY	100 Ω
		F1	45G7B1

Notes:

1 Resistors ±2%, capacitors ±5% unless otherwise stated.

2 F1 is a 4 pole crystal filter with a ±3.5kHz pass-band, implemented as a matched pair. The recommended part is from Golledge, however other parts may be equally suitable although matching arrangements will vary. When selecting and matching a crystal filter care should be taken to ensure a flat pass-band.

4.5 Power Supply Decoupling and Layout

The CMX990 has dual supply voltages: a 3.3V supply is required for the PLLs and charge pump circuits and for the digital I/O pads, and a 2.5V supply (with separate decoupling) is required for the RF sections (Rx1, Rx2, Tx) as well as the baseband analogue and digital circuits.

The 3.3V supply must be provided by an external regulator circuit. The 2.5V supply may be provided by an external regulator, or alternatively may be derived from the 3.3V supply using an off-chip low dropout transistor in conjunction with the on-chip control circuit (enabled by register PowerUp1 bit 5) - an example of this arrangement is shown in Figure 7. Whichever method is used to generate the 2.5V supply, the 2.5V regulator may be turned off while the CMX990 is quiescent in order to save power. The CMX990 will then allow the supply to drop to 2.0V, at which point it will be clamped by a separate on-chip micropower regulator. This is done so that the data in the on-chip registers and memories is not lost. The main 2.5V regulator circuit must be powered up again and allowed to settle before any RF or analogue circuitry, or the clock to the internal logic, is enabled. In other words, PowerUp1 (bits 7-6 and 4-0) and PowerUp2 (bits 7-4 and 0) must not be set high until the main 2.5V supply has been re-established.

The circuit shown in Figure 7 is an example, and will require that the 3.3V supply is regulated to within +/- 5%. This is necessary to ensure that the PNP transistor shown (TR3) does not enter saturation, taking worst case ambient conditions and bandgap / component tolerances into account.

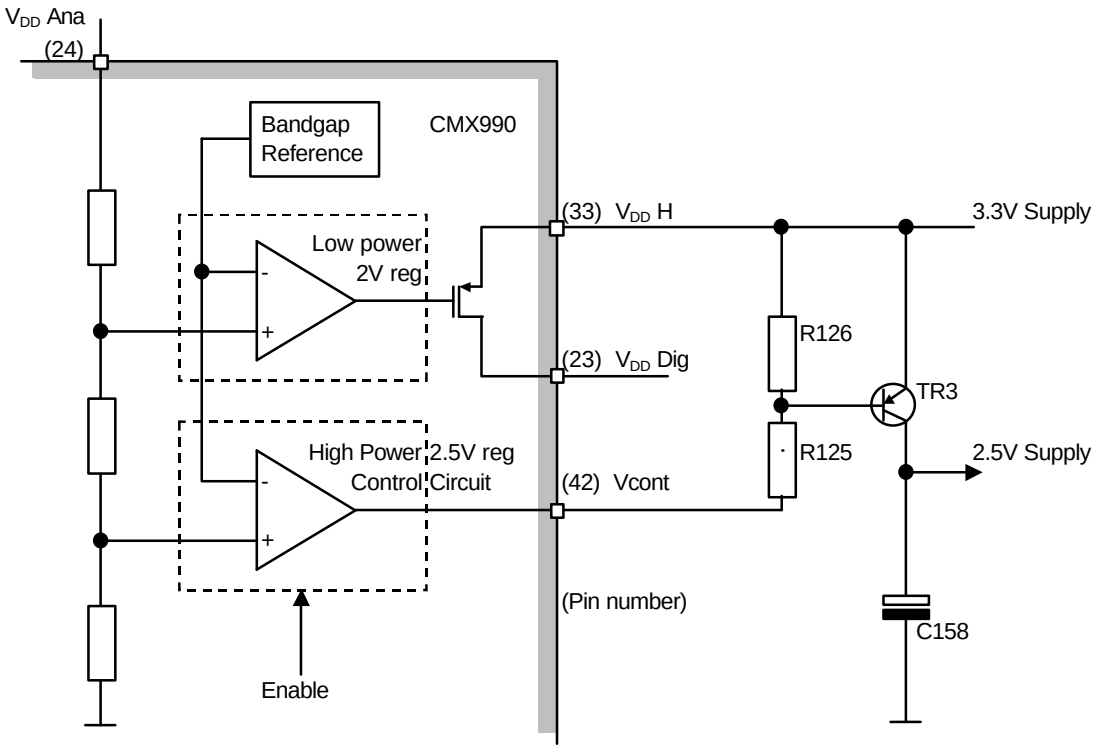


Figure 7 Voltage Regulator Connections

C158	100 µF	R125	330 Ω
TR3	PMBT4403	R126	47 kΩ

Resistors ±5%, capacitors and inductors ±20% unless otherwise stated.

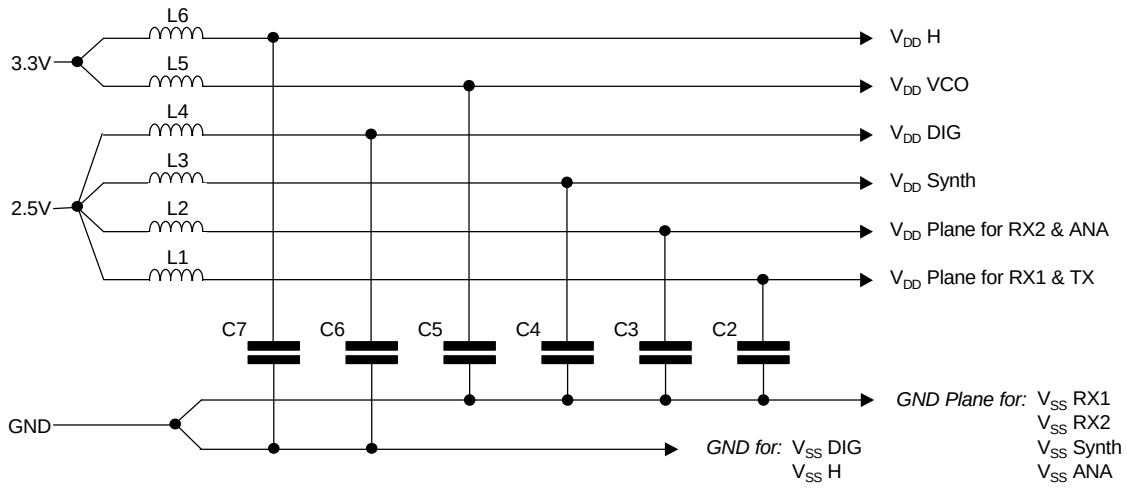


Figure 8 Power Supply Connections and De-coupling

C2	10 nF	L1	TBA
C3	10 nF	L2	TBA
C4	10 nF	L3	TBA
C5	10 nF	L4	TBA
C6	10 nF	L5	TBA
C7	10 nF	L6	TBA

Resistors ±5%, capacitors and inductors ±20% unless otherwise stated.

Layout Recommendations

To achieve good noise performance, decoupling of V_{BIAS} and all supplies is very important as is protection of the receive path from extraneous in-band signals. It is recommended that the printed circuit board is laid out with a ground plane in the CMX990 area to provide a low impedance connection between the V_{SS} pins and all V_{DD} and V_{BIAS} decoupling capacitors. As shown in Figure 8 the ground for V_{SS} digital signals should be kept separate from that used for analogue / RF signals. The digital ground should be routed back to a suitable star point.

The CMX990 package has a copper area connected to ground under the main body of the IC. This pad should be connected to analogue ground. It will be noted that caution should be exercised over placing any tracks underneath the CMX990. Further any vias other than ground should be avoided under the device unless manufacturers can guarantee that the exposed ground pad on the CMX990 will not cause shorts while a good electrical contact is maintained between the device and ground.

Apart from these recommendations normal RF layout practices should apply such as keeping tracks as short as possible, equal track lengths on differential inputs, care with coupling between tracks etc.

5. General Description

The CMX990 comprises a baseband modem and an associated RF section to provide the air-interface to the required Mobitex standard. Device control and status is transferred via a set of memory mapped registers. The following paragraphs provide a description of operation of each of the sections that make up the device.

The CMX990 is composed of 5 main sections:

5.1 Baseband modem

5.2 µC interface

5.3 Auxiliary ADC and DAC

5.4 Synthesiser

5.5 RF and IF

Each of the above will be described in its own section below:

5.1 Baseband Modem

This section has been designed to be compliant with the appropriate sections of the "Mobitex Interface Specification" including Short Block Frame formatting for the extended battery saving protocol. References to 'data blocks' in this section apply to both the normal (18 byte) Data Block and the smaller (4 byte) Short Data Block.

The function of this section is further divided into Receive and Transmit sections that operate in half duplex.

In transmit mode the data is encoded according to the Mobitex standard. This includes the calculation and appending of a Cyclic Redundancy Checksum (CRC) and Forward Error Correction (FEC), and Interleaving to reduce the effects of noise. The subsequent NRZ data stream is then filtered digitally and the resulting digital data processed to produce an I and Q signal as the baseband form of the required FM signal. These are converted to analogue signals via D-A converters and passed to the RF section for subsequent transmission.

In receive mode, the analogue I and Q representations, at baseband, of the FM signal from the RF section are converted to digital signals via A-D converters. These signals are digitally filtered to suppress the adjacent channels and demodulated digitally. The resulting signal is then filtered, to optimise the signal to noise performance, before slicing to resolve into a digital bit stream. Mobitex specified error correction and de-interleaving is applied and the resulting data is presented for transfer to an external processor.

5.1.1 Description of Blocks

Status and Data Quality Registers

8-bit registers which the µC can read to determine the status of the modem and the received data quality.

Command, Mode and Control Registers

The values written by the µC to these 8-bit registers control the operation of the modem.

Data Buffer

An 18-byte buffer used to hold receive or transmit data to or from the µC.

Frame Assembly / Disassembly

Each of these blocks consists of 4 circuits which generate (in transmit mode) or check (in receive mode) the bits of both short and normal Mobitex data blocks.

CRC Generator/Checker

A circuit which generates (in transmit) or checks (in receive) the CRC bits, which are included in transmitted Mobitex data blocks so that the receive modem can detect transmission errors.

FEC Generator/Checker

In transmit mode this circuit calculates and adds the FEC (4 bits) to each byte presented to it. In receive mode the FEC information is used to correct most transmission errors that have occurred in Mobitex data blocks or in the Frame Head control bytes.

Interleave/De-interleave Buffer

This circuit interleaves data bits within a data block before transmission and de-interleaves the received data block so that the FEC system is best able to handle short noise bursts or signal fades.

Scramble/De-scramble

This block may be optionally used to scramble/de-scramble the transmitted and received data blocks. It does this by modulating the data with a 511-bit pseudorandom sequence, as described in section 5.1.5.4. Scrambling improves the transmitted spectrum, especially when repetitive sequences are to be transmitted.

Frame Sync Detect

This circuit, which is only active in receive mode, is used to look for the user specified 16-bit Frame Synchronisation pattern which is transmitted to mark the start of every frame.

Tx Modulator and Low Pass Filter

The filter is used in transmit mode and is a low pass transitional Gaussian filter having a 3dB loss at 0.3 or 0.5 times the bit rate (BT=0.3 or 0.5). See figure 9. This filter eliminates the high frequency components which would otherwise cause interference into adjacent radio channels.

The unmodulated baseband 'eye' diagrams of the transmitted signal is shown in Figure 10.

The Tx Modulator converts the baseband signal into an I and Q form which is passed to the Tx IF stage.

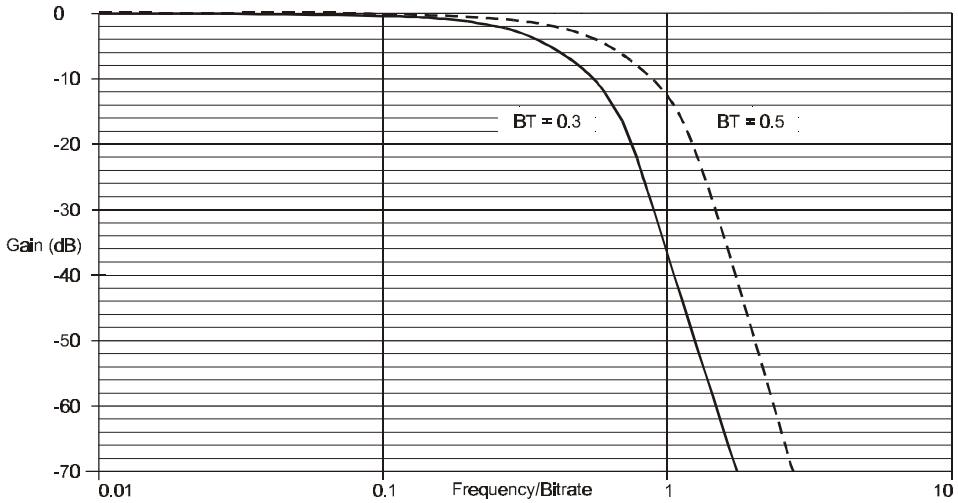


Figure 9 Typical Tx Baseband Filter Response

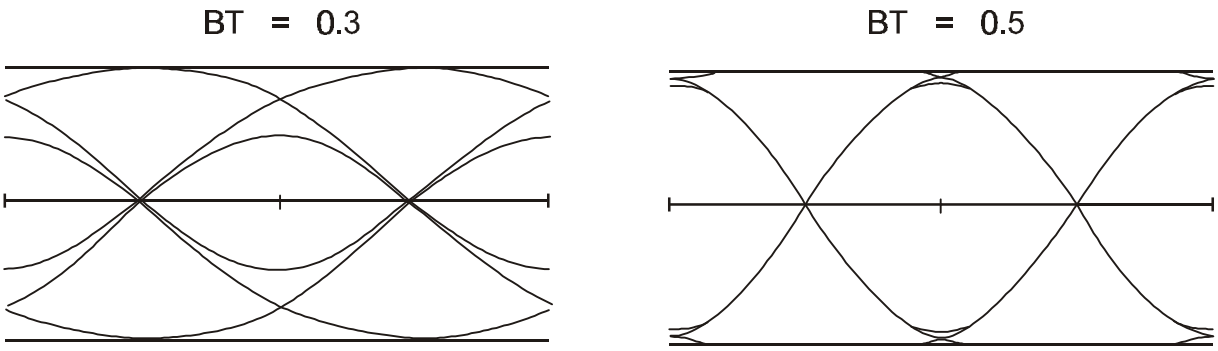


Figure 10 Baseband Transmitter Signal Eye Diagrams

Rx Low Pass Filter

This filter is a low pass transitional Gaussian filter having a 3dB loss at 0.56 times the bit rate (BT=0.56). It is used to reject HF noise to improve the BER.

Level Track and DPLL

These circuits, which operate only in receive mode, extract a bit rate clock from the received signal and measure the received signal amplitude and dc offset. This information is then used to extract the received bits and also to provide an input to the received Data Quality measuring circuit.

5.1.2 Modem - µC Interaction

In general, data is transmitted over air in the form of messages, or 'Frames', consisting of a 'Frame Head' optionally followed by one or more formatted data blocks. The Frame Head includes a Frame Synchronisation pattern designed to allow the receiving modem to identify the start of a frame. The following data blocks are constructed from the 'raw' data using a combination of CRC (Cyclic Redundancy Checksum) generation, Forward Error Correction coding, Interleaving and Scrambling. Details of the message formats handled by this modem are given in section 5.3.

To reduce the processing load on the host µC, this modem has been designed to perform as much as possible of the computationally intensive work involved in Frame formatting and de-formatting and (when in receive mode) in searching for and synchronising onto the Frame Head. In normal operation the modem will only require servicing by the µC once per received or transmitted data block.

Thus, to transmit a block, the host µC has only to load the unformatted (raw) binary data into the modem's data buffer then instruct the modem to format and transmit that data. The modem will then calculate and add the CRC bits as required, encode the result with Forward Error Correction coding, interleave then scramble the bits before transmission.

In receive mode, the modem can be instructed to assemble a block's worth of received bits, de-scramble and de-interleave the bits, check and correct them (using the FEC coding) and check the resulting CRC before placing the received binary data into the Data Buffer for the µC to read.

The modem can also handle the transmission and reception of unformatted data, to allow the transmission of special Bit and Frame Synchronisation sequences or test patterns.

5.1.3 Data Formats

Raw data
If required the user may transmit and receive raw data. This is transferred between the host and device a byte (8 bits) at a time.

Note that it is important to have established frame synchronisation before receiving data to enable the receiving device to decode synchronously. The user may add error detection and correction by way of algorithms performed on the host device.

General Purpose Formats
In a proprietary system the user may employ the data elements provided by this device to construct a custom, over-air data structure.

For example, 16 bits of bit sync + 2 bytes of frame sync + 4 bytes of receiver and sender address + n data blocks would be sent as:

TQB (bit and frame sync) + TQB (addresses) + (n x TDB) + TSB

And received as:

SFS + RSB + RSB + RSB + RSB + (n x RDB)

Mobitex Frame Structure
The Mobitex format for transmitted data is in the form of a Frame Head immediately followed by either 1 Short Data Block or a number of Data Blocks (0 to 32).

The Frame Head consists of 7 bytes:

2 bytes of bit sync:
1100110011001100 from base,
0011001100110011 from mobile
bits are transmitted from left to right

2 bytes of frame sync:
System specific.

2 bytes of control data.

1 byte of FEC code, 4 bits for each of the control bytes:
bits 7-4 (leftmost) operate on the first control byte.
bits 3-0 (rightmost) operate on the second control byte.

Each byte in the Frame Head is transmitted bit 7 (MSB) first to bit 0 (LSB) last.

The normal and short data blocks consist of:

18 bytes of data (Data Block) **OR** 4 bytes of data (Short Data Block).

2 bytes of CRC calculated from the data bytes.

4 bits of FEC code for each of the data and CRC bytes

The resulting data block bits are interleaved and scrambled before transmission.

Figure 11 shows how the over air signal is built up from Frame Sync and Bit Sync patterns, Control bytes and Data Blocks.

The binary data transferred between the modem and the host µC is that shown enclosed by the thick dashed rectangles near the top of the diagram.

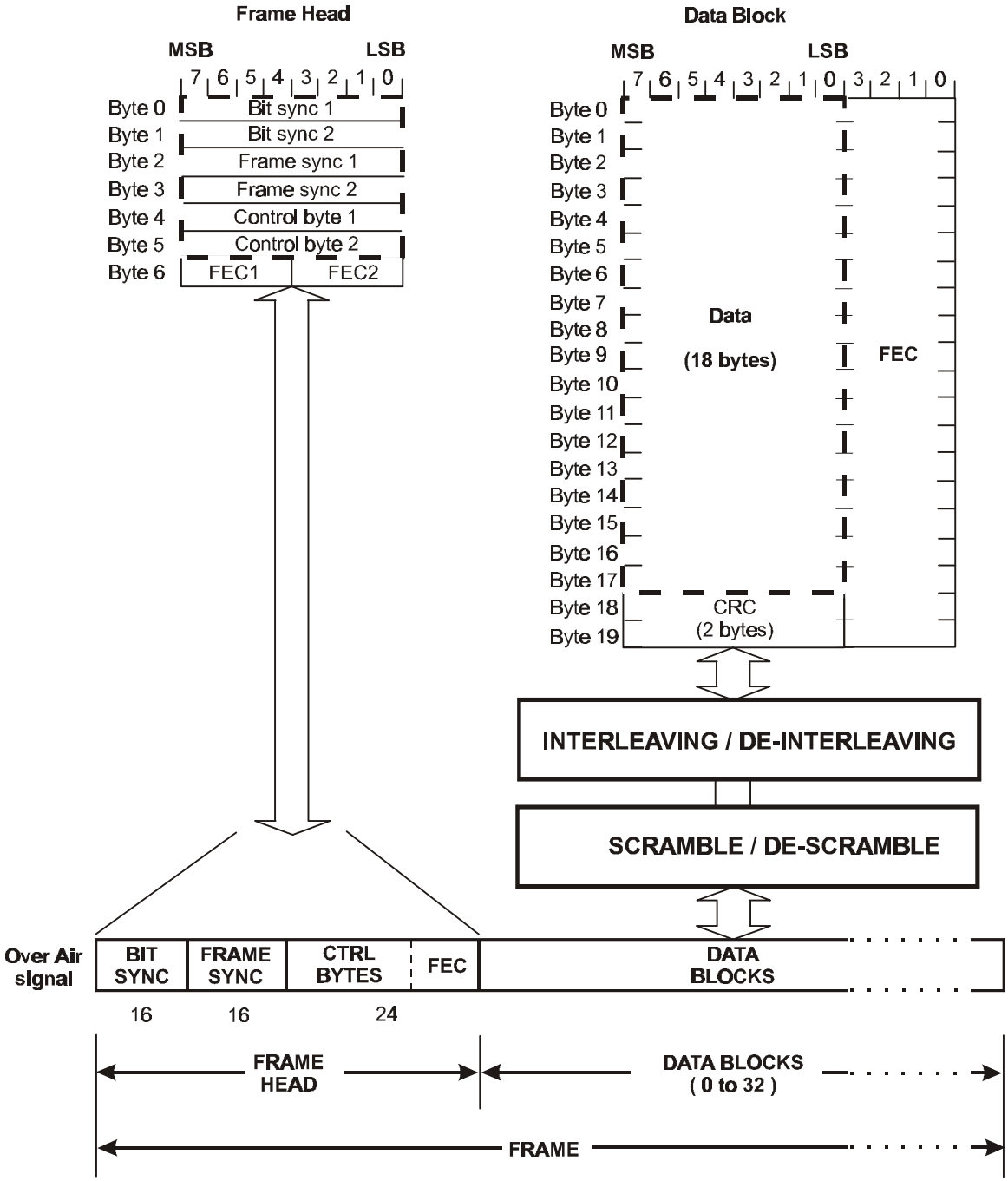


Figure 11 Mobitex Over Air Signal Format

5.1.4 Programmer's View of the Modem

The modem appears to the programmer as a series of 8-bit read and write registers, individual registers being selected by the A0 to A5 address pins. Most of the baseband control for formatting or decoding the data is controlled by the following registers:

Address	Write to Modem	Read from Modem
$00	Data Buffer	Data Buffer
$01	Command Register	Status 1 Register
$02	Control Register	Data Quality Register
$03	Mode Register	Status 2 Register

5.1.4.1 Data Buffer

This is an 18-byte read/write buffer which is used to transfer data (as opposed to command, status, mode, data quality and control information) between the modem and the host µC.

It appears to the µC as a single 8-bit register; the modem ensuring that sequential µC reads or writes to the buffer are routed to the correct locations within the buffer.

The µC should only access this buffer 2 µs after the Status Register BFREE (Buffer Free) bit is set to '1'.

The buffer should only be written to while in Tx mode and read from while in Rx mode (except when loading Frame Sync detection bytes while in Rx mode).

5.1.4.2 Command Register

Writing to this register tells the modem to perform a specific action or actions, depending on the setting of the TASK and acquire bits. The enable packet detect bit is used to indicate the presence of data signals in the receive path.

Command Register $01 Write

Bit:	7	6	5	4	3	2	1	0
	Acquire Bit Clock	Acquire I Q Offset	Acquire AFC	Enable packet detect	Task Control			

When it has no action to perform (but is not 'powersaved'), the modem will be in an 'idle' state. If the modem is in transmit mode the input to the Tx filter will be connected to a mid level. In receive mode the modem will continue to measure the received data quality and extract bits from the received signal, supplying them to the de-interleave buffer, but will otherwise ignore the received data.

Command Register B7: Acquire Bit Clock

This bit has no effect in transmit mode.

In receive mode, whenever a byte with the Acquire Bit Clock set to '1' is written to the Command Register, and TASK is not set to RESET, it initiates an automatic sequence designed to achieve bit timing synchronisation with the received signal as quickly as possible. This involves setting the Phase Locked Loop of the received bit timing extraction circuits to its widest bandwidth, then gradually reducing the bandwidth as timing synchronisation is achieved, until it reaches the 'normal' value set by the PLL Control bits of the Control Register.

Setting this bit to '0' (or changing it from '1' to '0') has no effect, however note that the acquisition sequence will be re-started every time that a byte written to the Command Register has the Acquire Bit Clock bit set to '1'. Details of the acquisition sequence are in section 5.1.4.3.

The Acquire Bit Clock will normally be set to '1' up to 12 bits before an SFS (Search for Frame Sync) or SFH (Search for Frame Head) task, however it may also be used independently to re-establish clock synchronisation quickly after a long fade. Alternatively, a SFS or SFH task may be written to the Command Register with the Acquire Bit Clock bit set to '0' if it is known that clock synchronisation does not need to be re-established. Details of the acquisition sequence are in section 5.1.4.3.

Command Register B6: Acquire I Q Offset

This bit has no effect in transmit mode.

In receive mode, when this bit is changed from a '0' to a '1' it initiates an automatic sequence designed to compensate the gross dc offset of the received I and Q signal. This sequence involves temporarily disabling the RF input and setting the analogue offset measurement circuits to compensate for the resulting I and Q dc offset. Once this has been completed the RF input will be reasserted and remaining I and Q offsets will be measured and compensated depending on the setting of bits 4 and 5 of the Control Register ($02).

Changing this bit from '1' to '0' will terminate acquisition and the 'normal' value set by bits 4 and 5 of the Control Register ($02) will be carried out.

The Acquire I Q Offset bit will normally be set after changing or reacquiring a channel (e.g. after powering up from a sleep condition). This would normally be done so the acquisition sequence was completed before an SFS or SFH task is initiated. Alternatively, a SFS or SFH task may be written to the Command Register without previously setting the Acquire I Q Offset bit to '1' if it is known that there is no need to re-establish the received signal offsets, e.g. when receiving another message on the same channel in quick succession. Details of the acquisition sequence are in section 5.1.4.3.

The error rate is highest immediately after an Acquire Bit Clock and Acquire I Q Offset sequence is triggered and rapidly reduces to its static value soon after. These erroneous bits could incorrectly trigger the frame sync detection circuits and so it is suggested that a SFH or SFS task is set 12 bits after setting the Acquire Bit Clock sequence and when the Acquire I Q Offset has completed.

Command Register B5: Acquire AFC

This bit has no effect in transmit mode.

In receive mode, when this bit is changed from a '0' to a '1' it initiates an automatic sequence designed to measure and compensate for small differences in the carrier frequencies of the transmitter and receiver. If the TCXO frequency is too far out the dc offset in the demodulated signal will become excessive and limit the decode performance of the device. In these cases the host must adjust the TCXO frequency via the on chip DAC based on the value read from the Frequency Offset register ($04).

In Mobitex systems the carrier frequencies of basestations are very accurate compared to the permitted tolerances of mobile units. Therefore once a mobile unit has set up it's local TCXO frequency it should be suitable for transmitting or receiving with any basestation. The Slow tracking mode should be sufficient to track any variations caused by environmental changes. Details of the acquisition sequence are in section 5.1.4.3.

Command Register B4: Enable packet detect

This bit has no effect in transmit mode.

In receive mode if this bit is set to '1' the device will monitor the demodulated waveform for signals likely to be valid data. The likely presence of valid data will be reported via bit 0 of Status Register 1. This information can assist in the timing of setting a SFS or SFH task. Note

that some noise signals may appear in the baseband as valid data, the RSSI signal should be used to confirm that the received signal is suitable before relying on this signal.

It is recommended that this bit is only set to '1' when searching for the start of a packet. Once a frame sync has been detected this bit should be set to '0' until the start of a new packet needs to be found.

Command Register B3, B2, B1, B0: Task

Operations such as transmitting a data block are treated by the modem as 'tasks' and are initiated when the µC writes a byte to the Command Register with the TASK bits set to one of the data handling commands (marked BOLD in the table below).

Mobitex modem tasks:

B3	B2	B1	B0	Receive Mode		Transmit Mode	
0	0	0	0	NULL		NULL	
0	0	0	1	**SFH**	Search for Frame Head	**T7H**	Transmit 7 byte Frame Head
0	0	1	0	**R3H**	Read 3 byte Frame Head		Reserved
0	0	1	1	**RDB**	Read Data Block	**TDB**	Transmit Data Block
0	1	0	0	**SFS**	Search for Frame Sync	**TQB**	Transmit 4 Bytes
0	1	0	1	**RSB**	Read Single Byte	**TSB**	Transmit Single Byte
0	1	1	0	**LFSB**	Load Frame Sync Bytes	**TSO**	Transmit Scrambler Output
0	1	1	1	RESET	Cancel any current action	RESET	Cancel any current action
1	0	0	1	**SFHZ**	SFH with zero errors		Reserved
1	0	1	1	**RSD**	Read Short Data Block	**TSD**	Transmit Short Data Block
1	1	0	0	**SFSZ**	SFS with zero errors		Reserved

Note: All other bit patterns are reserved.
Bold text indicates a 'data handling command'

The µC should not write a data handling command to the Command Register or write to or read from the Data Buffer when the BFREE (Buffer Free) bit of the Status 1 Register is '0'.

Different tasks apply in receive and transmit modes. Detailed timings for the various tasks are given in Figures 14 and 15.

Transmit Operation

When the modem is in transmit mode, all data handling commands other than TSO instruct the modem to transmit data from the Data Buffer, formatting it as required. For these tasks the µC should wait until the BFREE (Buffer Free) bit of the Status 1 Register is '1', before writing the data to the Data Buffer. If more than 1 byte needs to be written to the Data Buffer, byte number 0 of the block should be written first. The host should then write the desired task to the Command Register.

Once the byte containing the desired task has been written to the Command Register, the modem will:

Set the BFREE (Buffer Free) bit of the Status 1 Register to '0'.

Take the data from the Data Buffer as quickly as it can - transferring it to the Interleave Buffer for eventual transmission. This operation will start immediately if the modem is 'idle' (i.e. not transmitting data from a previous task), otherwise it will be delayed until there is sufficient room in the Interleave Buffer.

Once all of the data has been transferred from the Data Buffer the modem will set the BFREE and IRQ bits of the Status 1 Register to '1', (causing the chip IRQN output to go low if the IRQ Enable bit of the Mode Register has been set to '1') to tell the µC that it may write new data and the next task to the modem.

In this way the µC can write a task and the associated data to the modem while the modem is still transmitting the data from the previous task. See Figure 12.

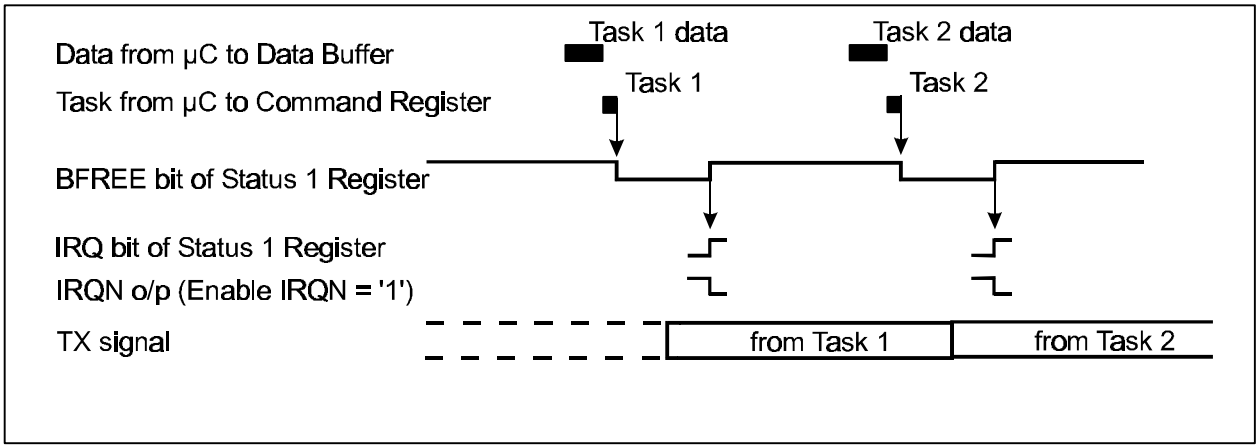


Figure 12 The Transmit Process

Receive Operation

When the modem is in receive mode, the µC should wait until the BFREE bit of the Status 1 Register is '1', then write the desired task to the Command Register.

Once the byte containing the desired task has been written to the Command Register, the modem will:

Set the BFREE bit of the Status Register to '0'.

Wait until enough received bits are in the De-interleave Buffer.

Decode them as needed, and transfer any resulting data to the Data Buffer.

Then the modem will set the BFREE and IRQ bits of Status 1 Register to '1', (causing the IRQN output to go low if the IRQ Enable bit of the Mode Register has been set to '1') to tell the µC that it may read from the Data Buffer and write the next task to the modem. If more than 1 byte is contained in the Data Buffer, byte number '0' of the data will be read first.

In this way the µC can read data and write a new task to the modem while the received bits needed for this new task are being stored in the De-interleave Buffer. See Figure 13.

The above is not true for loading the Frame Sync detection bytes (LFSB): the bytes to be compared with the incoming data must be loaded prior to the task bits being written.

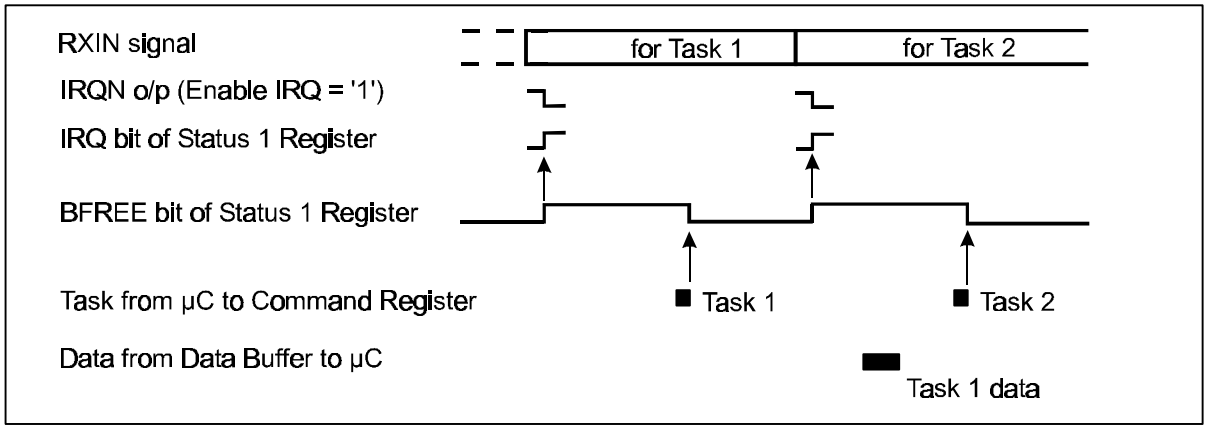


Figure 13 The Receive Process

Task Descriptions:

NULL - No effect

This task is provided so the acquisition commands can be issued without loading a new task.

SFH - Search for Frame Head

Causes the modem to search the received signal for a Frame Head. The Frame Head will consist of a 16-bit Frame Sync followed by control data (see Figure 11 - Mobitex Over Air Signal). The search will continue until a Frame Head has been found, or until the RESET task is loaded.

The search is carried out by first attempting to match the incoming bits against the previously programmed (task LFSB) 16-bit Frame Sync pattern (allowing up to any one bit (of 16) in error). When a match has been found, the modem will read the next 3 received bytes as Frame Head bytes, these bytes will be checked, and corrected if necessary, using the FEC bits. The two Frame Head Data bytes are then placed into the Data Buffer.

The BFREE and IRQ bits of the Status 1 Register will then be set to a logic '1' to indicate that the µC may read the 2 Frame Head Data bytes from the Data Buffer and write the next task to the Command Register. If the FEC indicates uncorrectable errors the modem will set the CRCFEC bit in the Status 1 Register to a logic '1'. The MOBAN bit (Mobile or Base) in the Status 1 Register will be set according to the polarity of the 3 bits preceding the Frame Sync pattern.

R3H - Read 3-byte Frame Head

This task, which would normally follow an SFS task, will place the next 3 bytes directly into the Data Buffer. It also causes the modem to check the 3 bytes as Frame Head control data bytes and will set the CRCFEC bit to a logic '1' (high) only if the FEC bits indicate uncorrectable errors. Note: This task will not correct any errors and, due to the Mobitex FEC specification, will not detect all possible uncorrectable error patterns. The BFREE and IRQ bits of the Status 1 Register will be set to '1' when the task is complete to indicate that the µC may read the data from the Data Buffer and write the next task to the modem's Command Register.

The CRCFEC bit in the Status 1 Register will be set according to the validity of the received FEC bits.

RDB - Read Data Block

This task causes the modem to read the next 240 bits as a Mobitex Data Block.

It will de-scramble and de-interleave the bits, FEC correct and CRC check the resulting 18 data bytes and place them into the Data Buffer, setting the BFREE and IRQ bits of the Status 1 Register to '1' when the task is complete to indicate that the µC may read the data from the Data Buffer and write the next task to the modem's Command Register. The CRCFEC bit will be set according to the outcome of the CRC check.

Note: in receive mode the CRC checksum circuits are initialised on completion of any task other than NULL.

SFS - Search for Frame Sync

This task, which is intended for special test and channel monitoring purposes, performs the first part only of a SFH task. It causes the modem to search the received signal for a 16-bit sequence which matches the Frame Synchronisation pattern with up to any 1 bit in error.

When a match is found the modem will set the BFREE and IRQ bits of the Status 1 Register to '1' and update the MOBAN bit. The µC may then write the next task to the Command Register.

RSB - Read Single Byte

This task causes the modem to read the next 8 bits and translate them directly (without de-interleaving or FEC) to a single byte which is placed into the Data Buffer (B7 will represent the earliest bit received). The BFREE and IRQ bits of the Status 1 Register will then be set to '1' to indicate that the µC may read the data byte from the Data Buffer and write the next task to the Command Register.

This task is intended for special tests and channel monitoring - perhaps preceded by an SFS task.

LFSB - Load Frame Sync Bytes

This task takes 2 bytes from the Data Buffer and updates the Frame Sync detect bytes. The MSB of byte '0' is compared to the first bit of a received Frame Sync pattern and the LSB of byte '1' is compared to the last bit of a received Frame Sync pattern. This task does not enable Frame Sync detection.

Unlike other Rx tasks, the data buffer must be loaded before the task is issued and the task must only be issued 'between' received messages, i.e. before the first task for receiving a message and after the last data is read out of the data buffer.

Once the modem has read the Frame Sync bytes from the Data Buffer, the BFREE and IRQ bits of the Status 1 Register will be set to '1', indicating to the µC that it may write the next task to the modem.

SFHZ - Search for Frame Head with Zero Errors

This performs the same task as SFH task but allowing no bits to be in error over the 16-bit Frame Sync pattern.

RSD - Read Short Data Block

This task causes the modem to read the next 72 bits as a Mobitex Short Data Block.

It will de-scramble and de-interleave the bits, FEC correct and CRC check the resulting 4 data bytes and place them into the Data Buffer, setting the BFREE and IRQ bits of the Status 1 Register to '1' when the task is complete to indicate that the µC may read the data from the Data Buffer and write the next task to the modem's Command Register. The CRCFEC bit will be set according to the outcome of the CRC check.

Note: in receive mode the CRC checksum circuits are initialised on completion of any task other than NULL.

SFSZ - Search for Frame Sync with Zero Errors

This performs the same task as SFS task but allowing no bits to be in error over the 16-bit Frame Sync pattern.

T7H - Transmit 7-byte Frame Head

This task takes 6 bytes of data from the Data Buffer, calculates and appends 8 bits of FEC from bytes '4' and '5' then transmits the result as a complete Mobitex Frame Head.

Bytes '0' and '1' form the bit sync pattern, bytes '2' and '3' form the frame sync pattern and bytes '4' and '5' are the frame head control bytes. Bit 7 of byte '0' of the Data Buffer is sent first, bit 0 of the FEC byte last.

Once the modem has read the data bytes from the Data Buffer, the BFREE and IRQ bits of the Status 1 Register will be set to '1', indicating to the µC that it may write the next task and its data to the modem.

TQB - Transmit 4 Bytes

This task takes 4 bytes of data from the Data Buffer and transmits them, bit 7 first.

Once the modem has read the data bytes from the Data Buffer, the BFREE and IRQ bits of the Status 1 Register will be set to '1', indicating to the µC that it may write the next task and its data to the modem.

TDB - Transmit Data Block

This task takes 18 bytes of data from the Data Buffer, calculates and applies a 16-bit CRC and forms the FEC for the 18 data bytes and the CRC. This data is then interleaved and passed through the scrambler, if enabled, before being transmitted as a Mobitex Data Block.

Once the modem has read the data bytes from the Data Buffer, the BFREE and IRQ bits of the Status Register will be set to '1', indicating to the µC that it may write the next task and its data to the modem.

Note: In transmit mode the CRC checksum circuit is initialised on completion of any task other than NULL.

TSB - Transmit Single Byte

This task takes a byte from the Data Buffer and transmits the 8 bits, bit 7 first.

Once the modem has read the data byte from the Data Buffer, the BFREE and IRQ bits of the Status 1 Register will be set to '1', indicating to the µC that it may write the next task and its data to the modem.

TSO - Transmit Scrambler Output

This task, intended for channel set-up, enables the scrambler and transmits its output.

When the modem has started the task the Status 1 Register bits will not change and hence these will not raise an IRQ. The µC may write the next task and its data to the modem at any time and the scrambler output will stop when the new task has produced its first data.

TSD - Transmit Short Data Block

This task takes 4 bytes of data from the Data Buffer, calculates and applies a 16-bit CRC and forms the FEC for the 4 data bytes and the CRC. This data is then interleaved and passed through the scrambler, if enabled, before being transmitted as a Mobitex Data Block.

Once the modem has read the data bytes from the Data Buffer, the BFREE and IRQ bits of the Status 1 Register will be set to '1', indicating to the µC that it may write the next task and its data to the modem.

Note: In transmit mode the CRC checksum circuit is initialised on completion of any task other than NULL.

RESET - Stop any current action

This task takes effect immediately, and terminates any current task the modem may be performing and sets the BFREE bit of the Status 1 Register to '1', without setting the IRQ bit. It should be used when V_{DD} is applied to set the modem into a known state.

Note that due to delays in the internal circuitry, it will take approximately 3 bit times for any change to become apparent at the transmitter output.

Task Timings

The device should not write to the Command Register whenever the Enable Baseband bit is changed from '0' to '1' and for at least 2 bit times after the following:

Changing the Tx/Rx bit.

Resetting or after power is applied to the device.

This is to ensure that the internal operation of the device is initialised correctly for the new task. Note that this only applies to the Command Register, the other registers may be accessed as normal.

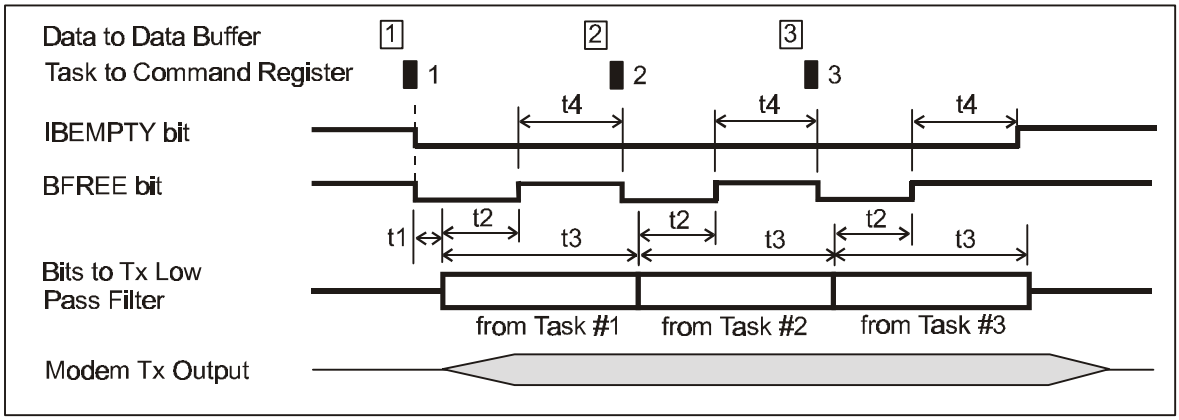


Figure 14 Transmit Mode Timing Diagram

		Task	Typical time (bit-times)
t1	Time from writing first task (modem in 'idle' state) to application of first transmit bit to Tx Low Pass filter	Any	1
t2	Time from application of first bit of task to Tx Low Pass filter until BFREE goes to a logic '1' (high)	T7H	36
		TQB	24
		TDB	20
		TSB	1
		TSD	6
t3	Time to transmit all bits of task	T7H	56
		TQB	32
		TDB	240
		TSB	8
		TSD	72
t4	Max time allowed from BFREE going to a logic '1' (high) for next task (and data) to be written to modem	T7H	18
		TQB	6
		TDB	218
		TSB	6
		TSD	64

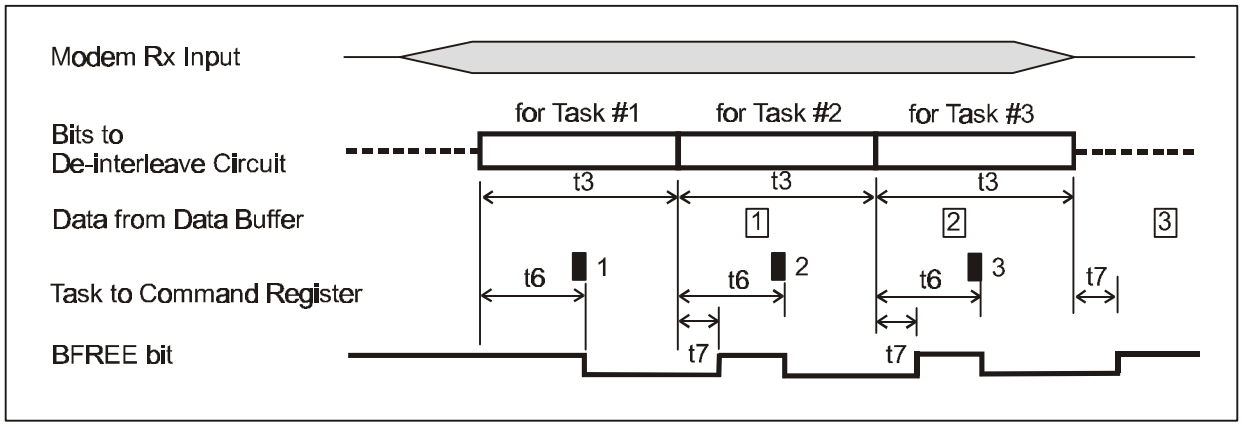


Figure 15 Receive Mode Timing Diagram

		Task	Typical time (bit-times)
t3	Time to receive all bits of task	SFH	56
		R3H	24
		RDB	240
		RSB	8
		RSD	72
t6	Maximum time between first bit of task entering de-interleave circuit and task being written to modem	SFH	14
		R3H	18
		RDB	218
		RSB	6
		RSD	64
t7	Time from last bit of task entering de-interleave circuit to BFREE going to a logic '1' (high)	Any	1

Tx and Rx Low Pass Filter Delay

The previous task timing figures are based on the signal at the input to the RF sections (in transmit mode) or the input to the de-interleave buffer (in receive mode). There is an additional delay of about 2 bit times in both transmit and receive modes due to the Tx/Rx filtering and RF circuitry, as illustrated in the figure below.

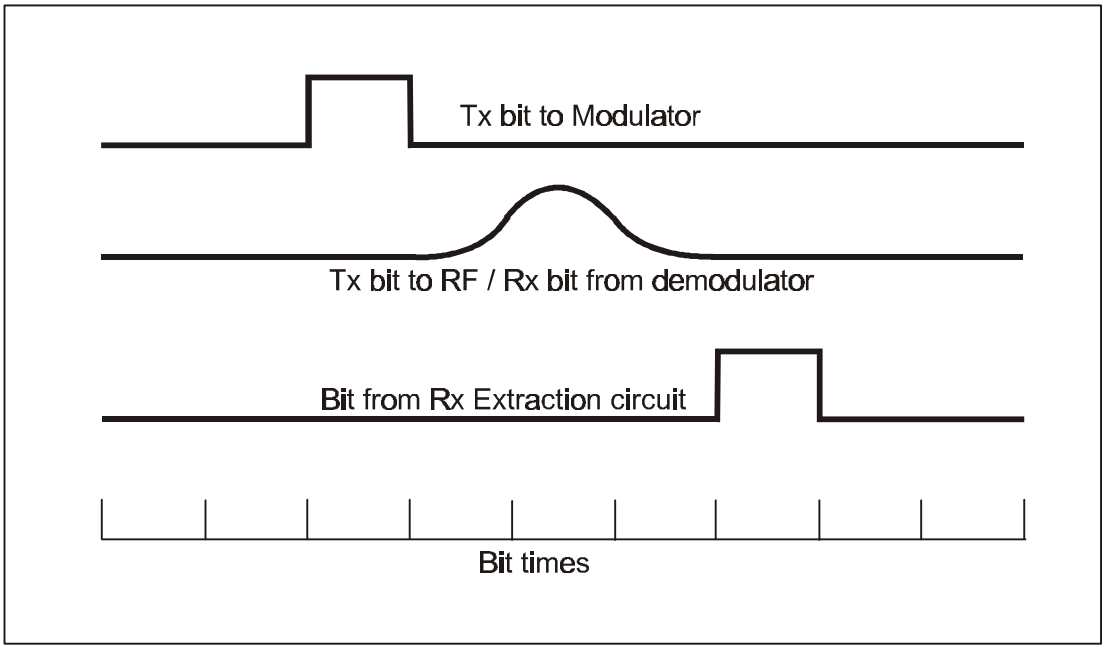


Figure 16 Low Pass Filter Delay

5.1.4.3 Control Register

This 8-bit write only register controls the response times of the receive clock extraction and signal level measurement circuits.

Control Register $02 Write

Bit:	7	6	5	4	3	2	1	0
	AGC Control		IQ Offset Control		Frequency tracking (AFC) Control		PLL Control	

The modem needs to make accurate measurements of the received signal level, dc offset and frequency offset and bit timing to achieve reasonable error rates. Accurate measurements, especially in the presence of noise, are best made by averaging over a relatively long time.

However, in most cases the modem will be used to receive isolated messages from a distant transmitter and may be turned on for a very short time before the message starts. Also, the received baseband signal out of the radio's frequency discriminator will have a dc offset due to small differences between the receiver and transmitter reference oscillators and hence their 'carrier' frequencies.

To cater for this situation acquire bits 7 to 5 are provided in the Command register ($01) which, when triggered, cause the modem to follow an automatic sequence designed to perform these measurements as quickly as possible. After these acquisition sequences have completed the circuits return to the mode as set in this register.

Control Register B7, B6: AGC Control

These two bits have no effect in transmit mode.

In receive mode these bits set the response of the AGC circuit. The 'Run' and 'Max Gain and Run' settings allow the circuit to acquire and track incoming signals.

B7	B6	Setting	Action
0	0	Max Gain and Hold	AGC set to maximum gain and held
0	1	Hold*	AGC gain not updated by internal circuit
1	0	Run	AGC tracks input signal
1	1	Max Gain and Run	AGC set to maximum gain and tracks input signal

* Host may override AGC setting by writing to $19 only when this setting is selected.

Control Register B5, B4: I/Q Offset Control

These two bits have no effect in transmit mode.

In receive mode, these set the 'normal' response of the I/Q offset measuring circuits. The offset control is in two sections, an analogue 'coarse' setting and a digital 'fine' setting. The host may read and directly overwrite the coarse setting via registers $18 and $19. The coarse and fine settings will be overridden by the Acquire I Q Offset command (bit 6 of Command register) which will go through a sequence of:

Reset
Run with Coarse Tracking for 12 bits to correct gross I/Q offset error
Run with Fine Tracking for 640 bits to adjust for remaining I/Q offsets
Revert to normal setting (hold / fine / coarse)

B5	B4	Setting	Action
0	0	Reset and Hold	I/Q offset tracking reset and held
0	1	Hold*	I/Q offset tracking held at current setting
1	0	Fine Tracking*	I/Q fine offset tracking
1	1	Coarse Tracking	I/Q coarse offset tracking

* Host may override Coarse I/Q Offset by writing to registers $18 and $19 only when these settings are selected and bit 6 of Command register is = '0'.

Control Register B3, B2: Frequency tracking (AFC) Control

These two bits have no effect in transmit mode.

In receive mode, they set the 'normal' response of the frequency tracking circuits. This setting will be temporarily overridden by the Acquire AFC command (bit 5 of Command register) which will go through a sequence of:

Reset
Run with Fast Tracking for 96 bits to correct frequency offset error
Run with Slow Tracking for 750 bits to follow any further frequency offsets
Revert to normal setting (hold / slow / fast)

B3	B2	Setting	Action
0	0	Reset and Hold	Frequency tracking reset and held
0	1	Hold	Frequency tracking held at current setting
1	0	Slow Tracking	Frequency slow tracking
1	1	Fast Tracking	Frequency fast tracking

For Mobitex systems, and most general purpose applications using the modem, these bits should normally be set to Slow Tracking after the host has activated the automatic sequence.

The Fast setting allows the modem to respond quickly without µC intervention - although at the cost of reduced Bit Error Rate versus Signal to Noise performance.

Note that the AFC measuring system requires '00' and '11' bit pairs to be received at reasonably frequent intervals. The AFC tracking will eventually fail if '1' or '0' is transmitted continuously.

Control Register B1, B0: PLL Control

These two bits have no effect in transmit mode.

In receive mode, they set the 'normal' bandwidth of the Rx clock extraction Phase Locked Loop circuit. This setting will be temporarily overridden by the Acquire Bit Clock command (bit 7 of Command register) which will go through a sequence depending if a frame sync is being searched for (SFH or SFS task is started within 14 bits):

Frame sync search:	*No frame sync search:*
Wide setting until Frame Sync is detected	16 bits of wide setting
30 bits of medium setting	30 bits of medium setting
Revert to normal setting	Revert to normal setting

B1	B0	PLL Bandwidth	Suggested use
0	0	Hold	Signal fades
0	1	Narrow	< ± 20ppm bit rate error systems
1	0	Medium	Wide bit rate error or long preamble acquisition
1	1	Wide	Quick acquisition

The 'hold' setting is intended for use during signal fades, otherwise the minimum bandwidth consistent with the transmit and receive modem bit rate tolerances should be chosen.

The wide and medium bandwidth settings allow the modem to respond rapidly to fresh messages and recover rapidly after a fade without µC intervention - although at the cost of reduced Bit Error Rate versus Signal to Noise performance.

Note that the clock extraction circuits work by detecting the timing of edges, i.e. a change from '0' to '1' or '1' to '0'. The clock extraction will eventually fail if '1' or '0' is transmitted continuously

5.1.4.4 Mode Register

The contents of this 8-bit write only register control the basic operating modes of the modem:

Mode Register $03 Write

Bit:	7	6	5	4	3	2	1	0
	IRQ Enable	INVBit	TxRxN	SCREn	En PLL Lock IRQ	Enable DQ IRQ	Enable Main ADC	Enable Main DAC

Mode Register B7: IRQ Enable - IRQN Output Enable

When this bit is set to '1' the IRQN chip output pin is pulled low (to V_{SS}) whenever the IRQ bit of the Status Register is a '1'.

Mode Register B6: INVBIT - Invert Bits

This bit controls inversion of transmitted and received data. This allows for frequency inversions in the RF chain and has the effect of swapping I and Q paths in both transmitter and receiver.

Mode Register B5: TXRXN - Tx/Rx Mode

Setting this bit to '1' puts the modem into Transmit mode, clearing it to '0' puts the modem into Receive mode. When changing from Rx to Tx there must be a 2-bit pause before setting a new task to allow the filter to stabilise. (See also Baseband Enable bit).

Note that changing between receive and transmit modes will cancel any current task. Note also that this bit does not enable Tx or Rx sections of the CMX990 which must be enabled by separate control bits.

Mode Register B4: SCREN - Scramble Enable

The scrambler only takes effect during the transmission or reception of a Mobitex Data Block, Short Data Block and during a TSO task. Setting this bit to '1' enables scrambling, clearing it to '0' disables scrambling.

The scrambler is only operative, if enabled by this control bit, during TSO, RDB, RSD, TSD or TDB, it is held in a reset state at all other times.

This bit should not be changed while the modem is decoding or transmitting a Mobitex Data Block.

Mode Register B3: En PLL Lock IRQ - Enable Phase Lock Loop lost IRQ

Setting this bit to '1' causes the IRQ bit of the Status 1 Register to be set to '1' whenever The PLL Lock lost bit is set to 1. (The Phase Lock lost bit of Status 2 Register will also be set to '1' at the same time.)

Mode Register B2: Enable DQ IRQ - Enable Data Quality IRQ

In receive mode, setting this bit to '1' causes the IRQ bit of the Status 1 Register to be set to '1' whenever a new Data Quality reading is ready. (The DQRDY bit of the Status 1 Register will also be set to '1' at the same time.)

In transmit mode this bit has no effect.

Mode Register B1 - 0: Enable Main ADC / Enable Main DAC

When the respective bit is set to '1' the main ADC and DAC are enabled, power may be saved by setting these bits to '0' when the ADC or DAC are not needed. Bit '0' would normally only be set to '1' when bit 5 is set to '1'. Bit '1' would normally only be set to '1' when bit 5 is set to '0'.

5.1.4.5 Status 1 Register

This register may be read by the µC to determine the current state of the modem.

Status 1 Register $01 Read

Bit:	7	6	5	4	3	2	1	0
	IRQ	BFREE	IBEMPTY	DIBOVF	CRCFEC	DQRDY	MoBaN	Packet Detect

Status 1 Register, B7: IRQ - Interrupt Request

This bit is set to '1' by:

The Status 1 Register BFREE bit going from '0' to '1', unless this is caused by a RESET task or by a change to the Mode Register Enable Baseband or TXRXN bits.

or The Status 1 Register IBEMPTY bit going from '0' to '1', unless this is caused by a RESET task or by changing the Mode Register Enable Baseband or TXRXN bits.

or The Status 1 Register DQRDY bit going from '0' to '1' (If DQEN = '1').

or The Status 1 Register DIBOVF bit going from '0' to '1'.

or The Status 1 Register Packet Detect bit going from '0' to '1' if the Enable Packet Detect bit is set in the Command Register.

or The Status 2 Register bits 7, 3, 2, 1 or 0 going from '0' to '1'.

The host must read Status 1 Register first after detecting or looking for an interrupt condition. The IRQ bit is cleared to '0' immediately after a read of the Status Register that caused the interrupt. In the case where 1 or more bits in Status 2 Register cause an interrupt the IRQ bit is only cleared after reading Status 2 Register.

If the IRQEN bit of the Mode Register is '1', then the chip IRQN output will be pulled low (to Vss) whenever the IRQ bit is '1'.

Status 1 Register, B6: BFREE - Data Buffer Free

This bit reflects the availability of the Data Buffer and is cleared to '0' whenever a task other than NULL, RESET or TSO is written to the Command Register.

In transmit mode, the BFREE bit will be set to '1' (also setting the Status 1 Register IRQ bit to '1') when the modem is ready for the µC to write new data to the Data Buffer and the next task to the Command Register.

In receive mode, the BFREE bit is set to '1' (also setting the Status 1 Register IRQ bit to '1') by the modem when it has completed a task and any data associated with that task has been placed into the Data Buffer. The µC may then read that data and write the next task to the Command Register.

The BFREE bit is also set to '1', but without setting the IRQ bit, by a RESET task or when the Mode Register Enable Baseband or TXRXN bits are changed.

Status 1 Register, B5: IBEMPTY - Interleave Buffer Empty

In transmit mode, this bit will be set to '1', also setting the IRQ bit, when less than two bits remain in the Interleave Buffer. Any transmit task written to the modem after this bit goes to '1' will be too late to avoid a gap in the transmit output signal.

The bit is also set to '1' by a RESET task or by a change of the Mode Register TXRXN or Enable Baseband bits, but in these cases the IRQ bit will not be set.

The bit is cleared to ‘0’ by writing a task other than NULL, RESET or TSO to the Command Register.

Note: When the modem is in transmit mode and the Interleave Buffer is empty, a mid-level voltage (V_{BIAS}) will be applied to the Tx low pass filter.

In receive mode this bit will be ‘0’.

Status 1 Register, B4: DIBOVF - De-Interleave Buffer Overflow

In receive mode this bit will be set to ‘1’ (also setting the IRQ bit) when a task is written to the Command Register too late to allow continuous reception.

The bit is cleared to ‘0’ by reading the Status 1 Register or by writing a RESET task to the Command Register or by changing the Enable Baseband or TXRXN bits of the Mode Register.

In transmit mode this bit will be ‘0’.

Status 1 Register, B3: CRCFEC - CRC or FEC Error

In receive mode this bit will be updated at the end of a Mobitex Data Block task, after checking the CRC, and at the end of receiving Frame Head control bytes, after checking the FEC. A ‘0’ indicates that the CRC was received correctly or the FEC did not find uncorrectable errors, a ‘1’ indicates that errors are present.

The bit is only cleared to ‘0’ by a RESET task or by changing the Enable Baseband or TXRXN bits of the Mode Register.

In transmit mode this bit will be ‘0’.

Status 1 Register, B2: DQRDY - Data Quality Reading Ready

In receive mode, this bit is set to ‘1’ whenever a Data Quality reading has been completed.

The bit is cleared to '0' after reading the Data Quality Register.

Immediately after a RESET task, or a change in the Enable Baseband or TXRXN bits to ‘0’, the DQRDY bit may be set and generate an interrupt. The value in the Data Quality Register will not be valid in this case.

Status 1 Register, B1: MOBAN - Mobile or Base Bit Sync Received

In receive mode this bit is updated at the end of the SFS and SFH tasks. This bit is set to ‘1’ whenever the 3 bits immediately preceding a detected Frame sync are ‘011’ (received left to right), with up to any one bit in error. The bit is set to ‘0’ if the bit pattern is ‘100’, again with up to any one bit in error. Thus, if this bit is set to ‘1’ then the received message is likely to have originated from a Mobile and if it is set to ‘0’ from a Base Station.

In transmit mode this bit is a logic ‘0’.

Status Register 1, B0: Packet Detect

This bit indicates the status of the Packet Detect circuit and will be set to '0' when a packet is not present, as described in the description for Command Register bit B4.

In transmit mode this bit will be ‘0’.

5.1.4.6 Data Quality Register

Data Quality Register $02 Read

Bit:	7	6	5	4	3	2	1	0
	Data Quality Reading (0-255)							

This is intended to indicate the quality of the receive signal during a Mobitex Data Block or 30 single bytes. In receive mode, the modem measures the 'quality' of the received signal by comparing the actual received zero crossing time against an internally generated time. This value is averaged over 240 bits and at the end of the measurement the Data Quality Register and the DQRDY bit in the Status 1 Register is updated. Note: An interrupt will only occur at this time if the Enable DQ IRQ bit = '1'.

To provide synchronisation with Data Blocks, and hence ensure the Data Quality Register is updated in preparation to be read when the RDB task finishes, the measurement process is reset at the end of tasks SFH, SFS, RDB and R3H.

In transmit mode all bits of the Data Quality Register will be '0'.

Figure 17 shows how the value (0-240) read from the Data Quality Register varies with received signal to noise ratio.

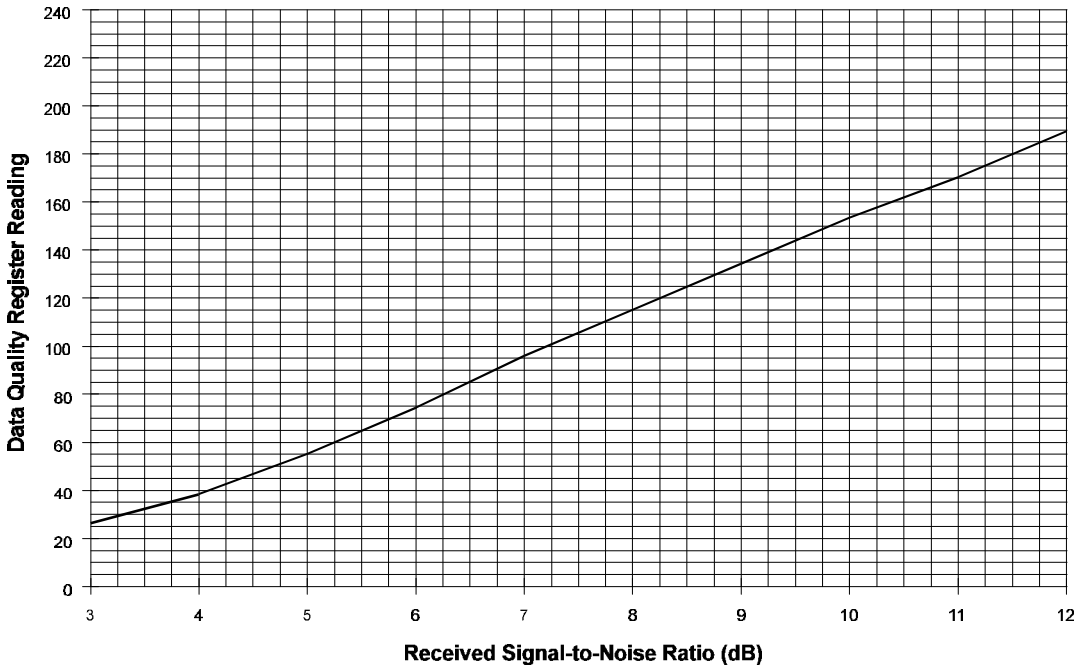


Figure 17 Typical Data Quality Reading (after 240 bits) vs baseband S/N (noise in bit rate bandwidth)

5.1.5 CRC, FEC, Interleaving and Scrambling Information:

5.1.5.1 CRC

This is a 16-bit CRC code used in both the Mobitex Data Block and Short Data Block. In transmit it is calculated by the modem from the data block bytes using the following generator polynomial:

$$g(x) = x^{16} + x^{12} + x^5 + 1$$

i.e. CRC - CCITT X.25.

This code detects all (single) error bursts of up to 16 bits in length and about 99.998% of all other error patterns.

The CRC register is initialised to all '1s' and the CRC is calculated octet by octet starting with the least significant bit of 'byte 0'. The CRC calculated is bit-wise inverted and appended to the data bytes with the most significant bit transmitted earliest.

In receive mode, a 16-bit CRC code is generated from the data bytes of each Mobitex Data Block or Short Data Block as above and the bit-wise inverted value is compared with the received CRC bytes. If a mis-match is present, then an error has been detected.

5.1.5.2 FEC

In transmit mode, during T7H, TSD and TDB, the modem generates a 4-bit Forward Error Correction code for each coded byte. The FEC is defined by the following H matrix:

	7_____0	3___0
	11101100	1000
H =	11010011	0100
	10111010	0010
	01110101	0001

Generation of the FEC consists of logically ANDing the byte to be transmitted with bits 7 to 0 of each row of the H matrix. Even parity is generated for each of the 4 results and these 4 parity bits, in the positions indicated by the last 4 columns of the H matrix, form the FEC code.

In checking the FEC, the received 12-bit word is logically ANDed with each row of the H matrix (earliest bit received compared with the first column). Again even parity is generated for the 4 resulting words and these parity bits form a 4-bit nibble. If this nibble is all zero then no errors have been detected. Other results 'point' to the bit in error or indicate that uncorrectable errors have occurred.

This code can correct any single error that has occurred in each 12-bit (8 data + 4 FEC) section of the message.

Example:
If the byte to be coded is '00101100' then the FEC is derived as follows:

H matrix row:	1	2	3	4
A	11101100	11010011	10111010	01110101
B	00101100	00101100	00101100	00101100
A AND B	00101100	00000000	00101000	00100100
Even Parity:	1	0	0	0

where A is bits 7 - 0 of one row of the H matrix and B is the byte to be coded. The even parity bits apply to the result of 'A AND B'.

So the word formed will be: '00101100 1000' sent left to right

When the same process is carried out on these 12 bits as above, using all 12 bits of each H matrix row, the resulting 4 parity bits will be '0000'.

5.1.5.3 Interleaving

All the bits of transmitted Mobitex Data Blocks and Short Data Blocks are interleaved by the modem to give protection against noise bursts and short fades. Interleaving is not performed on any bits in the Mobitex Frame Head.

In the Mobitex Data Block case, considering the 240 bits to be numbered sequentially before interleaving as 0 to 239 ('0' = bit 7 of byte 0, '11' = bit 0 of FEC for byte 0, ... , '239' = bit 0 of FEC for byte 19 - see Figure 6), then they will be transmitted as shown in Figure 13. The Mobitex Short Data Block is interleaved in a similar way; referring to Figure 13 consider bytes 4 and 5 as the CRC data and ignore bits 72 to 239 in the lower part of the diagram. i.e. the last bit to be transmitted will be '71'.

The modem performs the inverse operation (de-interleaving) in receive mode on both Mobitex Data Blocks and Short Data Blocks.

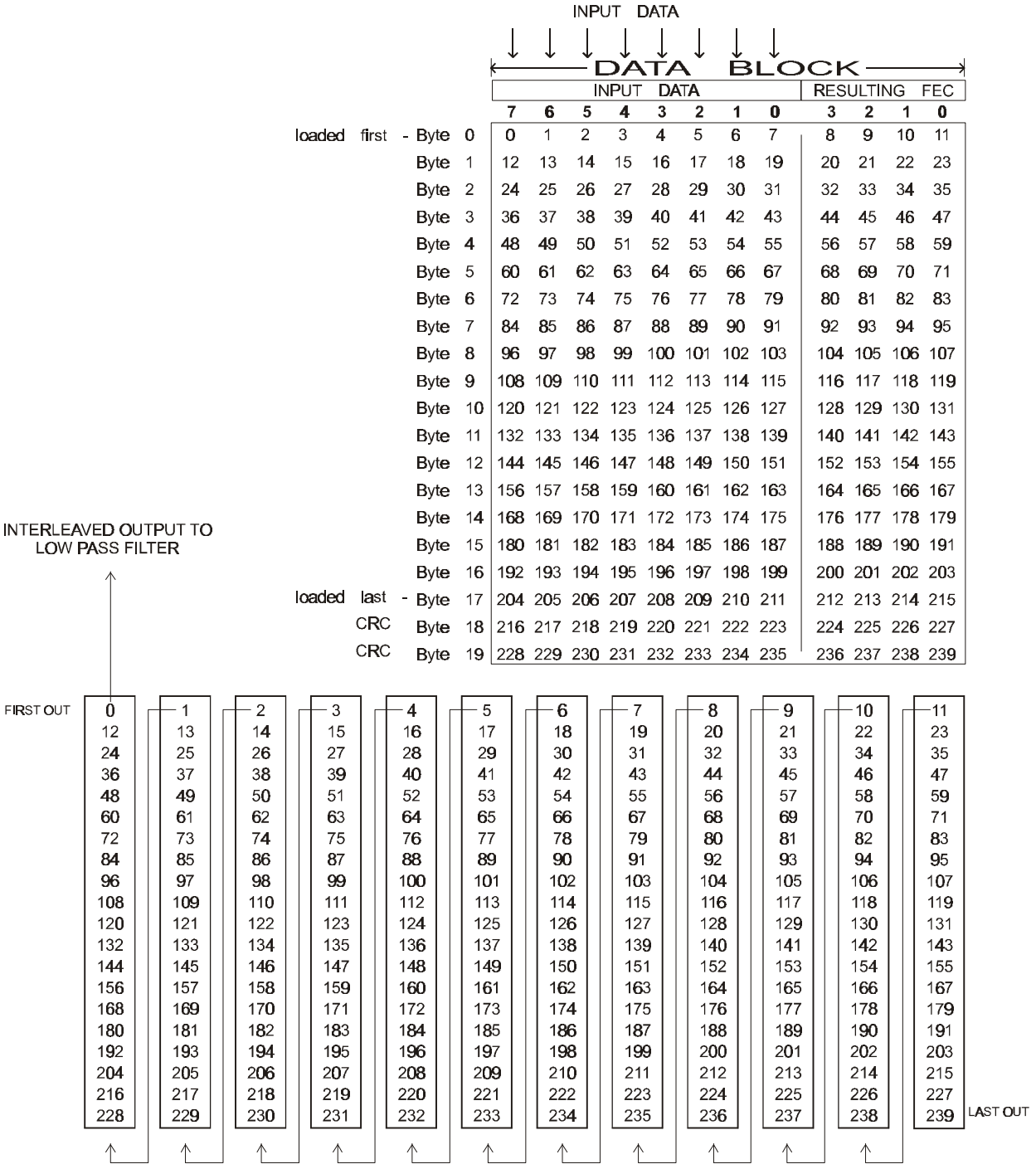


Figure 18 Interleaving - Input/Output

5.1.5.4 Scrambling

All formatted bits of both Mobitex Data Blocks and Short Data Blocks are XORed with the output of a 9-bit scrambler. This scrambler is initialised at the beginning of the first data block in every Frame. The 511-bit sequence is generated with a 9-bit shift register with the output of the 5th and 9th stages XOR'ed and fed back to the input of the first stage. The scrambler is disabled during all other tasks, apart for TSO.

5.1.6 Application Notes

5.1.6.1 Transmit Frame Example

If the device is required to send a Mobitex Frame the following control signals and data should be issued to the modem, assuming the device is not starting from a powersave state, TXRXN is set to '1' and that the relevant control bits have been set as required after power was applied to the device:

1. 6 bytes forming the Frame Head are loaded into the Data Buffer, followed by a 2-bit pause to let the filter stabilise, followed by setting T7H task.
2. Device interrupts host µC with IRQN when the 6th byte is read from the Data Buffer.
3. Status Register is read and 18 bytes are loaded, followed by setting TDB task.
4. Device interrupts host µC with IRQN when 18th byte is read from the Data Buffer.
5. Status 1 Register is read, host may load data and set next task as required:

   GOTO '1' if the last Data Block for this Frame has been transmitted and another Frame is to be immediately transmitted
   GOTO '3' if another Data Block in this Frame is to be transmitted
   GOTO '6' if no more data is to be immediately sent

6. 1 byte representing the 'hang byte' is loaded into the Data Buffer, followed by setting the TSB task.

If the 'hang byte' has been transmitted and no more data is to be sent then a new task need not be written and the µC can wait for the IBEMPTY interrupt when, after a few bits to allow for the Tx filter delay, it can shut down the Tx RF circuits.

A top level flowchart of the transmit process is shown in Figure 19.

Hang Byte

The filtering required to reduce the transmitted bandwidth causes energy from each bit of information to be smeared across 3 bit times. To ensure that the last bit transmitted is received correctly it is necessary to add an 8-bit 'hang byte' to the end of each message. Thus the tasks required to transmit an isolated Mobitex frame are:

$$T7H + (n \times TDB) + TSB$$

When receiving this data, the extra byte can be ignored as its only function is to ensure integrity of the last bit and not to carry any information itself.

It is suggested that a '00110011' or '11001100' pattern is used for this 'hang byte'.

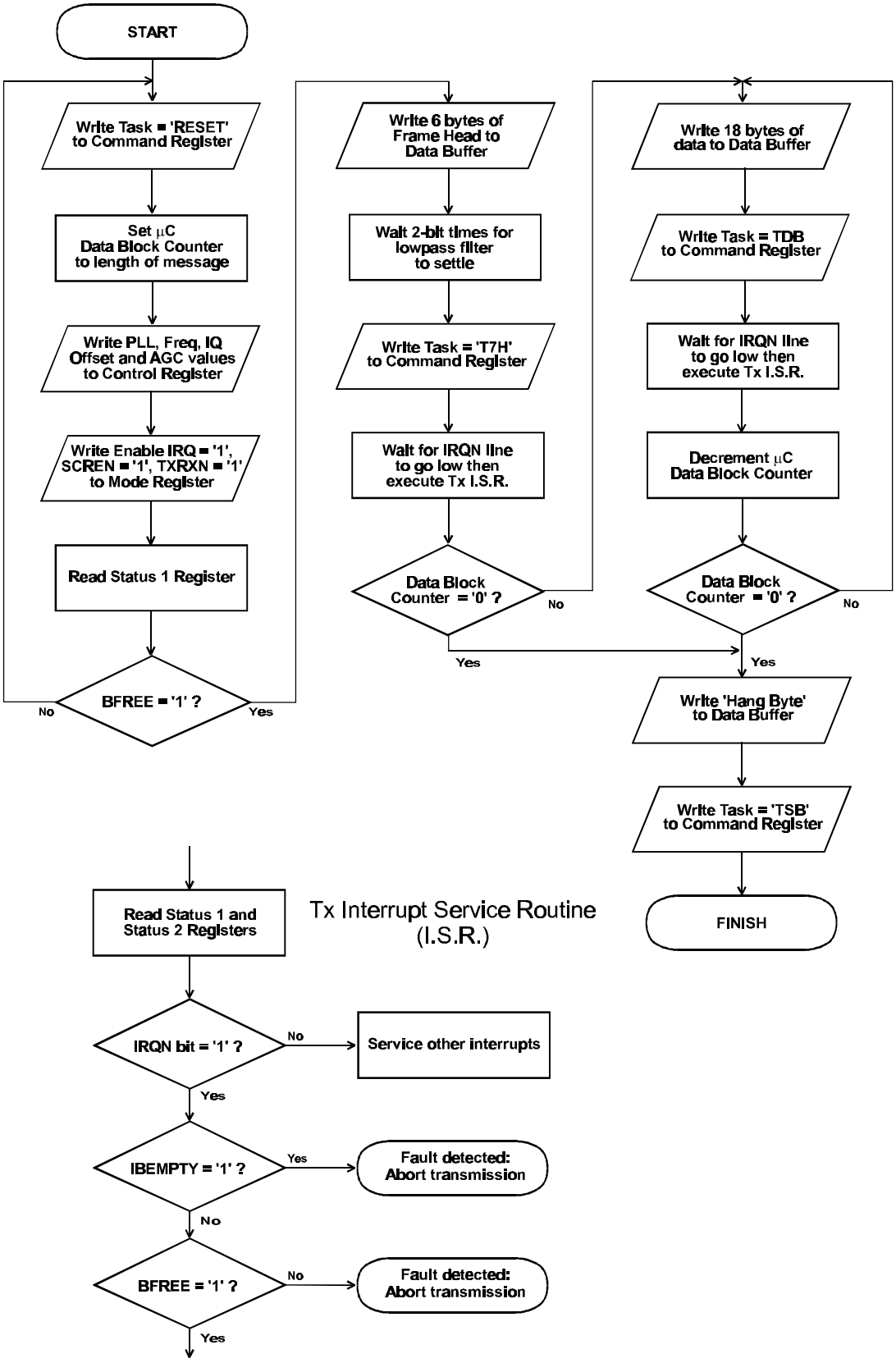


Figure 19 Transmit Process

5.1.6.2 Receive Frame Example

If the device is required to decode a Mobitex Frame the following control signals should be issued to the modem. The host should set the Control Register and activate the Acquire I Q Offset and Acquire AFC each time a new channel is selected when the RSSI indicates a valid signal or carrier only is present before packets are decoded. This also assumes that the device is initially not in powersave, the SCREN is set as required, TXRXN bit is set to '0' and a Packet Detect event has occurred, or a Frame Head is imminently expected:

1. 2 Frame Sync bytes are loaded.
2. 2 bits after the carrier has been detected, a LFSB task is loaded, along with setting the Acquire Bit Clock to initiate the bit clock extraction sequence.
3. Device interrupts host µC with IRQN when 2nd byte is read from Data Buffer.
4. Status Register is read, 12 bits later task is set to SFH to search for a Mobitex Frame Head.
5. Device will interrupt host µC with IRQN when valid Frame Sync is detected and header bytes decoded.
6. Host µC reads Status 1 Register, checks MOBAN and CRCFEC bit and reads out 2 Frame Head control bytes.
7. Host µC disables Packet Detect and sets the task to RDB to receive a Mobitex Data Block.
8. Device will interrupt host µC with IRQN when the Data Block has been received and the CRC has been calculated.
9. Host µC reads Status 1 Register, checks CRC validity and reads 18 Data Block bytes. The Data Quality Register can also be read to obtain the received S/N level.
10. Host µC sets task if more information is expected:

    GOTO '4' if last Data Block and another Frame Head imminently expected.
    GOTO '7' if another Mobitex Data Block expected.

If the last Data Block has been decoded and no more information is expected then the task bits need not be set as the device will automatically select the idle state.

A top level flowchart of the receive process is shown in Figure 20.

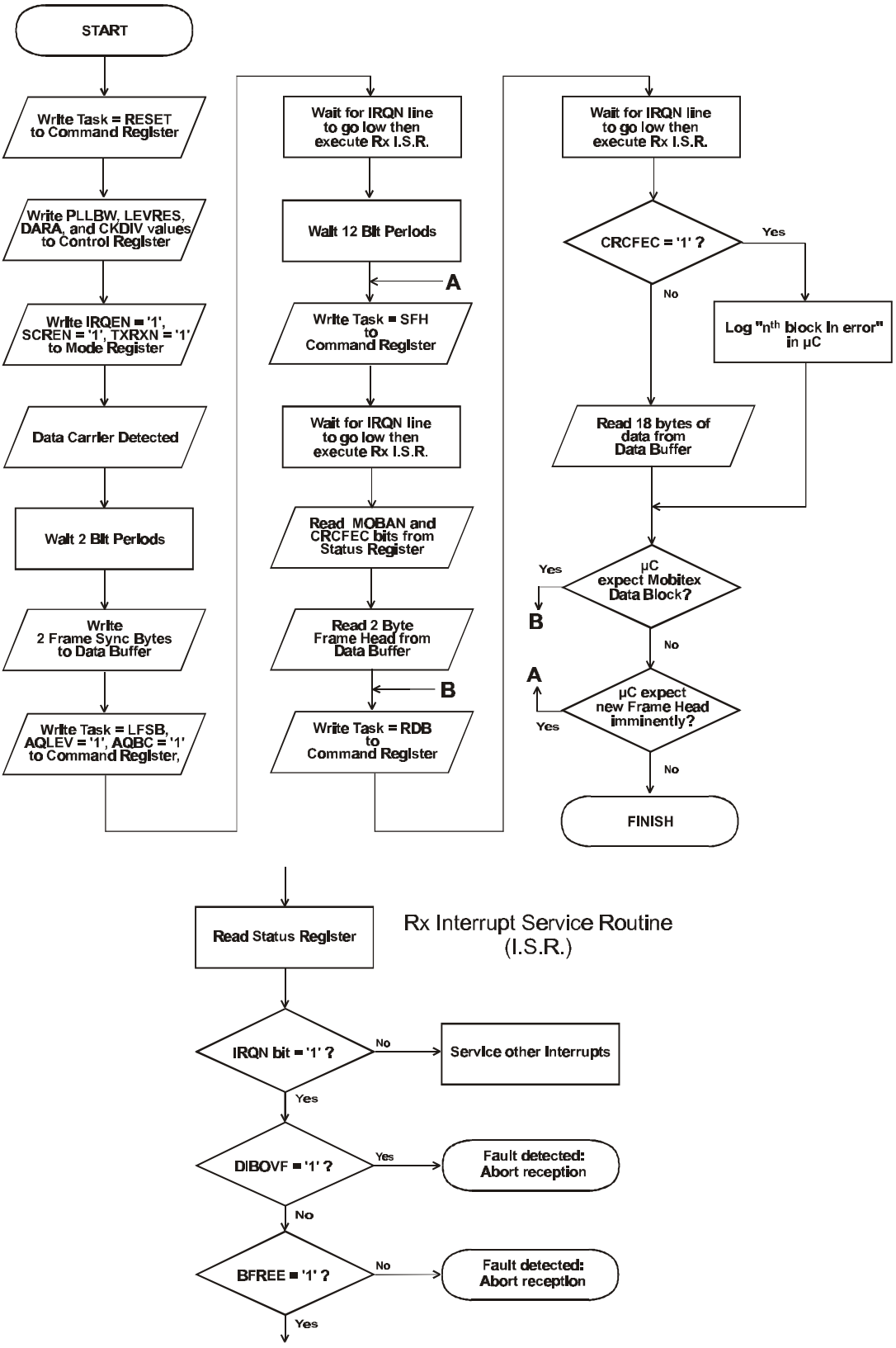


Figure 20 Receive Process

5.2 µC Interface

5.2.1 Memory Map and Interface

The following is a summary of the internal registers as seen by the host, details of operation may be found in the relevant section.

Address	Read	Write
$00	Data Buffer (Rx)	Data Buffer (Tx)
$01	Status 1	Command
$02	Data Quality	Control
$03	Status 2	Mode
$04	Freq Offset	Power Up 1
$05	RSSI	Power Up 2
$08	Aux ADC 0 LSB	Aux DAC 0 LSB
$09	Aux ADC 0 MSB	Aux DAC 0 MSB
$0A	Aux ADC 1 LSB	Aux DAC 1 LSB
$0B	Aux ADC 1 MSB	Aux DAC 1 MSB
$0C	Aux ADC 2 LSB	Aux DAC 2 LSB
$0D	Aux ADC 2 MSB	Aux DAC 2 MSB
$0E	Aux ADC 3 LSB	Aux DAC 3 LSB
$0F	Aux ADC 3 MSB	Aux DAC 3 MSB
$10	Aux ADC 4 LSB	RAM DAC control
$11	Aux ADC 4 MSB	Aux ADC control 1
$12	Aux ADC 5 LSB	Aux ADC control 2
$13	Aux ADC 5 MSB	-
$14	-	Aux Ram Data1 LSB
$15	-	Aux Ram Data1 MSB
$16	-	Aux Ram Data2 LSB
$17	-	Aux Ram Data2 MSB
$18	Analogue Setup 1	Analogue Setup 1
$19	Analogue Setup 2	Analogue Setup 2
$1A	-	Special Command
$1B	Special Data0 LSB	Special Data0 LSB
$1C	Special Data0 MSB	Special Data0 MSB
$1D	Special Data1 LSB	Special Data1 LSB
$1E	Special Data1 MSB	Special Data1 MSB
$20	-	Main PLL M div LSB
$21	-	Main PLL M div MSB
$22	-	Main PLL N div LSB
$23	-	Main PLL N div NSB
$24	-	Main PLL N div MSB
$25	-	Aux PLL M div LSB
$26	-	Aux PLL M div MSB
$27	-	Aux PLL N div LSB
$28	-	Aux PLL N div MSB
$TBA		Clock Control

Note: All unused addresses from $00 to $3F are reserved for future use.

Data Bus Buffers
The circuitry driving the D0-7 pins consists of 8 internal bidirectional 3-state logic level buffers between the internal registers and the external data bus lines.

Address and R/W Decode
Transfer of data bytes between the µC and the internal registers is controlled according to the state of the Write and Read Enable inputs (WRN and RDN), the Chip Select input (CSN) and the Register Address inputs A0 to A5.

The Data Bus Buffers, Address and R/W Decode blocks provide a byte-wide parallel µC interface, which can be memory-mapped, as shown in Figure 2.

5.2.2 Power-on and Reset

When power is first applied to the device an internal circuit will reset internal registers to '0' and put all circuit blocks in an inactive and power saved state.

Read bits will be reset to '0' - the inactive state. Counters / states will be reset to an inactive and known condition after a reset event - which can occur asynchronously.

Setting the RESET bit to '1' is similar except the RESET bit does not control the 'V Reg', 'Preserve registers' and 'Vbias' bits, they will remain at the last programmed state, as shown in bold in the following 2 register diagrams.

Power control

The following registers control individual power-up state of the indicated blocks. Note: Other sections of the device have the power control bits included in the control registers for those blocks. Blocks are disabled and in the zero power state when the associated control bit is '0'.

Power Up 1 $04 Write

Bit:	7	6	5	4	3	2	1	0
	Enable Clock	Enable Baseband	**V Reg**	Enable OP1 OP2	Rx IF	Rx RF1	Rx RF2	Tx RFIF

If the Enable Clock is set to '0' the on chip clock buffer will be disabled, the clock buffer must be enabled if setting RESET (bit 3 of $05) or if any of the internal circuits are powered up apart from those controlled by the 'V Reg', 'Vbias' and 'OP1 OP2' bits.

The Enable Baseband bit controls the data packeting and clock extraction circuits.

If V Reg bit is set to '0' an internal circuit will hold the nominal 2.5V supply pins at approximately 2V for data retention only. For normal operation the host must set this bit to '1' before enabling any other circuitry. If an external supply provides the nominal 2.5V then the V Reg bit should be set to '0'. See section 4.5 for more details.

When the OP1 OP2 bit is low both OP 1 and OP 2 amplifiers are disabled the OP1T and OP2T pins will become high impedance inputs to ADC2 and ADC3 respectively. When set to ‘1’ both op-amps are enabled.

Rx IF bit enables the circuitry from the IF IN pin to the differential I and Q outputs to the baseband.

Rx RF1 bit enables the circuitry from the RF IN A and RF IN B pins to the output of the 1st mixers.

Rx RF2 bit enables the circuitry from the output of the 1st mixers to the IF OUT pin.

Tx RFIF bit enables all the transmit RF and IF circuits from the differential I and Q inputs to the Tx RF interface pins.

Power Up 2 $05 Write

Bit:	7	6	5	4	3	2	1	0
	AUX DAC3	AUX DAC2	AUX DAC1	AUX DAC0	RESET	LNA ON (External)	**Preserve Registers**	**Vbias**

The Vbias control bit must be enabled early enough so that the output is stable before any of the other circuit blocks are enabled as this circuit takes some time to stabilise after being enabled. Setting the RESET bit to '1' will not change the Vbias bit.

If set to '1' the Preserve Registers bit will preserve most user settings programmed via the Special Command register, e.g. Rx channel filter coefficients and non assigned memory. In Rx mode the AGC, offsets and timing estimates of the received signal will be lost after a RESET event.

LNA ON bit directly controls the LNA ON pin and does not control any internal analogue circuitry. Any time delay for the external circuitry to stabilise must be taken into account when controlling this bit. This control bit will be cleared to '0' after a power on reset or if the RESET bit is set to '1'.

Whenever a '1' is written to the RESET bit all registers will be cleared to '0' apart from the Clock Control register, bit 5 of the Power Up 1 register and bits 1 and 0 of the Power Up 2 register. This will put all internal circuits in an inactive and power saved state. The 'V Reg', 'Preserve registers' and 'Vbias' bits will be unchanged. To ensure a clean exit from the RESET condition the RESET bit should be set to '0' before any other circuitry is enabled. i.e. To enter RESET write '000010xx' to $05. To exit RESET write '000000xx' then 'xxxx0xxx', where 'x' is the desired condition for the Aux DACs, LNA ON, 'Preserve registers' and 'Vbias' bits. The host may then program the rest of the device to the desired configuration.

The AUX DAC0-3 bits control the relevant auxiliary D2A converter.

5.2.3 Clock Control

The Ref Clock input can be divided down and then multiplied up to the required frequency to give the desired bit rate. Note: The reference for the synthesizers is the Ref Clock input to the device. The following table gives examples for common bit rates:

Ref clock (MHz)	Ref Clock Division	Base clock (MHz)
4.8	2	2.4
12	5	2.4
14.4	5	2.88
16.8	7	2.4
19.2	8	2.4
21.6	9	2.4

Base clock (MHz)	Base clock multiplier	Baseband clock (MHz)	Bit rate
2.4	4	9.6	4000
2.4	8	19.2	8000
2.4	16	38.4	16000
2.88	4	11.52	4800
2.88	8	23.04	9600

The Ref clock input to the device must be in the range 3.8MHz to 24MHz.
The Base Clock resulting from the division of the Ref Clock must be in the range 1.9MHz to 3.0MHz.

Clock Control $TBA Write

Bit:	7	6	5	4	3	2	1	0
	Base clock multiplier, 2 - 16 (0000 = x16, 0001 = Illegal state)				Ref Clock division, 2 - 16 (0000 = /16, 0001 = Illegal state)			

Notes: 1) To program '16' the host should load '0000', the value '0001' for both the above values should not be programmed.
2) The baseband clock will not be available for TBAms after exiting Reset.

5.2.4 Status Registers

Two status registers indicate events that may require action by the host. Those marked as bold in the diagrams below will cause bit 7 of Status1 (IRQ) to go high when they change from a 0 to 1. Interrupts are enabled by setting bit 7 of the Mode register ($03) to '1', the IRQN pin will then be pulled low whenever the IRQ bit goes high. If the IRQN line to the host is pulled low or if the host is polling for interrupts then Status Register 1 should be read first then optionally followed by reading Status Register 2. The IRQ bit will be cleared to a '0' when the status register containing the interrupt(s) is read.

Status1 $01 Read

Bit:	7	6	5	4	3	2	1	0
	IRQ	**BFREE**	**IBEMPTY**	**DIBOVF**	CRCFEC	**DQRDY**	MoBaN	**Packet Detect**

See section 5.1.4.5 for a description of Status register 1.

Status2 $03 Read

Bit:	7	6	5	4	3	2	1	0
	PLL Lock lost	Main PLL in lock	Aux PLL in lock	Tx PLL in lock	**SPC command complete**	**Aux ADC conversion complete**	**Freq offset error**	**IQ offset complete**

'PLL Lock lost' bit will be set to '1' whenever bits 4, 5 or 6 go from '1' to '0' since that bit was read as a '1' from Status Register 2, i.e. PLL Lock lost bit is only set if lock has been gained, the host has read the register to confirm this and that bit subsequently goes from a '1' to a '0'. This will cause bit 7 of Status1 to be set to '1' only if bit 3 of the Mode register ($03) is set to '1'. This bit will be cleared to '0' immediately after reading the Status 2 register.

Bits 6 to 4 represent the lock status for the corresponding PLL at the time of the read of Status 2 register. A '1' indicates the PLL is in lock, a '0' indicates that the PLL is not in lock. Buffer circuitry will prevent changes in the lock status being lost while this register is being read.

When operating a special command the 'SPC command complete' bit will be set to '1' when a command has finished and any associated data can then be read out. The correct sequence to initiate a special command is to load any required data into the special data registers $1B to $1E then issue the special command by writing to the special command register $1A. Having issued a special command the host must not read or write to the special command or data registers ($1A to $1E) until it has completed. Reading register Status 2 will clear this bit to '0'.

'Aux ADC conversion complete' bit will be set to '1' when all enabled ADC channels have been converted. This bit will not be set if continuous conversion is selected, the host may read the latest conversion for each channel as required. Reading register Status 2 will clear this bit to '0'.

During Rx mode the CMX990 continuously compares the local reference clock frequency against the received RF signal frequency. If these 2 frequencies deviate by more than the limit set by the host, the frequency offset error bit will be set to '1'. This bit will be cleared to '0' by reading register Status 2. By default the error limit is set so that this bit never gets set. This default value can be changed by issuing a special command to the CMX990 (see section 5.2.4).

'IQ offset complete' bit will be set to '1' when the sequence to estimate the IQ offsets of the receive channel has completed. During the offset acquisition sequence the received signal will be unreliable.

5.2.5 Write Only Registers

Data Buffer $00 Write

Bit:	7	6	5	4	3	2	1	0
	Tx Data							

Command Register $01 Write

Bit:	7	6	5	4	3	2	1	0
	Acquire Bit Clock	Acquire I Q Offset	Acquire AFC	Enable packet detect	Task Control			

Control Register $02 Write

Bit:	7	6	5	4	3	2	1	0
	AGC Control		IQ Offset Control		Frequency Tracking Control		PLL Control	

Mode Register $03 Write

Bit:	7	6	5	4	3	2	1	0
	IRQ Enable	INVBit	TxRxN	SCREn	En PLL Lock IRQ	Enable DQ IRQ	Enable Main ADC	Enable Main DAC

Power Up 1 $04 Write

Bit:	7	6	5	4	3	2	1	0
	Enable Clock	Enable Baseband	V Reg	OP1 OP2	Rx IF	Rx RF1	Rx RF2	Tx RFIF

Power Up 2 $05 Write

Bit:	7	6	5	4	3	2	1	0
	AUX DAC3	AUX DAC2	AUX DAC1	AUX DAC0	RESET	LNA ON (External)	Preserve Registers	Vbias

Aux DAC 0 $08-09 Write

Bit:	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	MSB								0	0	0	0	0	0	LSB	

Aux DAC 1 $0A-0B Write

Bit:	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	MSB								0	0	0	0	0	0	LSB	

Aux DAC 2 $0C-0D Write

Bit:	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	MSB								0	0	0	0	0	0	LSB	

Aux DAC 3 $0E-0F Write

Bit:	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	MSB								0	0	0	0	0	0	LSB	

RamDac control $10 Write

Bit:	7	6	5	4	3	2	1	0
	Inc Aux RAM address	En Aux RAM access	RAM DAC scan rate [0-7 = /1024 to /8]			Scan direction	En auto cycle	En RAM DAC

Aux Control1 $11 Write

Bit:	7	6	5	4	3	2	1	0
	0	0	Enable ADC 5	Enable ADC 4	Enable ADC 3	Enable ADC 2	Enable ADC 1	Enable ADC 0

Aux Control2 $12 Write

Bit:	7	6	5	4	3	2	1	0
	DAC RAM Polarity	Reset DAC RAMs	0	0	0	Conversion rate	Enable cont conversion	Start conversion

AuxRamData1 $14-15 Write

Bit:	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	MSB								0	0	0	0	0	0	LSB	

AuxRamData2 $16-17 Write

Bit:	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	MSB								0	0	0	0	0	0	LSB	

Analogue Setup 1 $18 Write

Bit:	7	6	5	4	3	2	1	0
	Set Tx attenuation: '11' = 10dB, '10' = 15 '01' = 25, '00' = 35		Coarse Rx I offset, '10000' = Mid value '00000' = Max -ve offset, '11111' = Max +ve offset					

Analogue Setup 2 $19 Write

Bit:	7	6	5	4	3	2	1	0
	Set Rx AGC: '11' = +40, '10' = +25 '01' = +10, '00' = -5dB		Coarse Rx Q offset, '10000' = Mid value '00000' = Max -ve offset, '11111' = Max +ve offset					

Special Command $1A Write

Bit:	7	6	5	4	3	2	1	0
	Special Command							

Special Data0 $1D-1E Read and Write

Bit:	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	MSB Data								LSB Data							

Special Data1 $1B-1C Read and Write

Bit:	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	MSB Data								LSB Data							

Main PLL M divider $20-21 Write

Bit:	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	Main PLL Enable	Tx LO DIV	0	MSB					LSB							

Main PLL N divider $22-23-24 Write

Bit:	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	Sign	0	0	0	MSB				NSB								LSB							

Aux PLL M divider $25-26 Write

Bit:	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	Aux PLL Enable	Tx IF Filter		MSB					LSB							

Aux PLL N divider $27-28 Write

Bit:	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	TX IF DIV	0	MSB						LSB							

Special Command (SPC) $1A Write

Bit:	7	6	5	4	3	2	1	0
	Special Command							

The 8 bit value written to this register instructs the modem to perform special tasks such as loading coefficients or reading receive values. When executing a special task that requires input data, the data should be loaded into the Special Data0/1 registers before writing the special command. When the special command has completed the 'SPC command complete' bit will be set to '1' and the host can read out any reply data from the Special Data0/1 registers. Note: When the internal circuits read this register as a non zero value they will attempt to complete the task when there is a gap in processing.

Function	Cmd No. (Hex)	Input Data		Returned Data		Notes
		Data 1 $1B $1C	Data 0 $1D $1E	Data1 $1B $1C	Data 0 $1D $1E	
Null	00	-	-	-	-	No command - do nothing
Set address	01	-	address	-	-	address1 = address
Set tx filter	09	-	-	-	-	address1 = tx filter address
Set rx channel filter	0A	-	-	-	-	address1 = rx channel filter address
Set rx gauss	0B	-	-	-	-	address1 = rx gauss filter address
Poke(addr)	0C	data	address	-	-	*address=data
Peek(addr)	0D	-	address	-	*address	
Branch	0E	-	address	-	-	Branches to address
Enter setup	11	-	-	-	-	Enters setup (debug code only)
Enter setup and wait	12	-	-	-	-	Enters setup (debug code only) synced to sample clk
Exit setup	13	-	-	-	-	Returns to tx/rx
Exit setup and initialise	14	-	-	-	-	Returns to tx/rx & initialises
User channel filter	15	-	-	-	-	Loads rx channel filter from data at address1
Set BT = 0.3	1A	-	-	-	-	Tx and Rx with BT = 0.3 (Default setting)
Set BT = 0.5	1B	-	-	-	-	Tx and Rx with BT = 0.5
Set AFC limit	1C		Limit			
Set Decode Threshold	18	-	Offset	-	-	Set data decode threshold level. Default = 2400

Notes: *address = data in memory pointed to by 'address'.

5.2.6 Read Only Registers

Data Buffer $00 Read

Bit:	7	6	5	4	3	2	1	0
	Rx Data							

Status1 $01 Read

Bit:	7	6	5	4	3	2	1	0
	IRQ	**BFREE**	**IBEMPTY**	**DIBOVF**	CRCFEC	**DQRDY**	MoBaN	**Packet Detect**

Data Quality Register $02 Read

Bit:	7	6	5	4	3	2	1	0
	Data Quality Reading (0-255)							

Status2 $03 Read

Bit:	7	6	5	4	3	2	1	0
	PLL Lock lost	Main PLL in lock	Aux PLL in lock	Tx PLL in lock	**SPC command complete**	**Aux ADC conversion complete**	**Freq offset error**	**IQ offset complete**

Frequency Offset $04 Read

Bit:	7	6	5	4	3	2	1	0
	Rx measured RF frequency offset (-64 to 63)							Good Data

The 2's complement number read from bits 7 to 1 represents the estimate of the frequency error between the transmitter and receiver carriers and is equivalent to 16Hz per bit, this value is only valid if bit 0 = '1'. If bit 0 = '0' the RF frequency offset will not be computed and bits 7 to 1 will hold the last value calculated.

Signal Strength $05 Read

Bit:	7	6	5	4	3	2	1	0
	Rx measured signal strength RSSI (0-255)							

The value read from this register represents the latest estimate of the RSSI as the number of dB above a level of -150 dB (to be confirmed).

Aux ADC 0 $08-09 Read

Bit:	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	MSB								X	X	X	X	X	X	LSB	

Aux ADC 1 $0A-0B Read

Bit:	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	MSB								X	X	X	X	X	X	LSB	

Aux ADC 2 $0C-0D Read

Bit:	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	MSB								X	X	X	X	X	X	LSB	

Aux ADC 3 $0E-0F Read

Bit:	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	MSB								X	X	X	X	X	X	LSB	

Aux ADC 4 $10-11 Read

Bit:	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	MSB								X	X	X	X	X	X	LSB	

Aux ADC 5 $12-13 Read

Bit:	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	MSB								X	X	X	X	X	X	LSB	

Analogue Setup 1 $18 Read

Bit:	7	6	5	4	3	2	1	0
	X	Channel filter overflow	Coarse Rx I offset, '10000' = Mid value '00000' = Max -ve offset, '11111' = Max +ve offset					

Bit 6 is set to '1' when the receive channel filters have a numerical overflow. This bit is reset to '0' after this register is read. This bit does not generate an interrupt and is intended for test purposes only for evaluating custom receive filter coefficients. Bits 5 to 0 indicate the current coarse offset correction in the receive I path.

Analogue Setup 2 $19 Read

Bit:	7	6	5	4	3	2	1	0
	AGC setting 0-3		Coarse Rx Q offset, '10000' = Mid value '00000' = Max -ve offset, '11111' = Max +ve offset					

Bits 7 to 6 indicate the current gain setting of the AGC circuit. Bits 5 to 0 indicate the current coarse offset correction in the receive Q path.

5.3 Auxiliary DAC and ADC

5.3.1 Aux DAC 0-3 $08-0F Auxiliary DAC Data Registers (Write only)

$08-09	Aux DAC 0	Auxiliary DAC 0 Data Register LSB - MSB
$0A-0B	Aux DAC 1	Auxiliary DAC 1 Data Register LSB - MSB
$0C-0D	Aux DAC 2	Auxiliary DAC 2 Data Register LSB - MSB
$0E-0F	Aux DAC 3	Auxiliary DAC 3 Data Register LSB - MSB

$08, $0A, $0C, $0E

Bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	DAC Data [1:0]	

$09, $0B, $0D, $0F

Bit	7	6	5	4	3	2	1	0
	DAC Data [9:2]							

There are two input registers for each of the four auxiliary DACs. Writing to the LSB register writes the two least significant bits of DAC data. Writing to the MSB register writes the eight most significant bits of DAC data and then passes all ten bits to the appropriate DAC input. If the MSB register is written while the LSB register is left constant, the converter may be treated as an 8-bit DAC.

5.3.2 RamDac Control $10 Auxiliary RAM DAC Control Register

Bit:

7	6	5	4	3	2	1	0
Inc Aux RAM address	En Aux RAM access	RAM DAC scan rate [0-7 = /1024 to /8]			Scan direction	En auto cycle	En RAM DAC

Setting bit 7 high will cause read operations to the auxiliary DAC RAM to increment the address pointer. Setting this bit low causes write operations to increment the address pointer.

Bit 6 enables access to the auxiliary DAC RAM. Setting bit 6 low resets the RamDac address pointer.

Bits 5 to 3 control the rate at which the RAM DAC address pointer changes:

Bit 5	Bit 4	Bit 3	Rate of change
0	0	0	MCLK/1024
0	0	1	MCLK/512
0	1	0	MCLK/256
0	1	1	MCLK/128
1	0	0	MCLK/64
1	0	1	MCLK/32
1	1	0	MCLK/16
1	1	1	MCLK/8

Bit 2 controls the direction of the memory scan operation. Setting this bit high will cause the memory address pointer to increment to the top location, setting this bit low will cause the memory address pointer to decrement to the bottom location. If this bit is changed while the

memory is being scanned, the current scan will complete before the new state of this bit takes effect.

When bit 1 is set high, the memory address pointer continuously increments to the top location and then decrements to the bottom location.

Bit 0 controls whether DAC0 is driven by the RAM (when set high) or the Aux DAC 0 register (when set low).

5.3.3 AuxRamData1/2 $14-17 Auxiliary DAC Memory I/O Access Addresses

$14

Bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	RAM data [1:0]	

$15

Bit	7	6	5	4	3	2	1	0
	RAM data [9:2]							

$16

Bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	RAM data [1:0]	

$17

Bit	7	6	5	4	3	2	1	0
	RAM data [9:2]							

These four address locations allow access to the 64 x 10-bit RAM. The contents of this RAM can be pre-loaded with a table of values that can be automatically sent to the auxiliary DAC0 in either a single cycle or continuous mode. Therefore the RAM can be used in conjunction with DAC0 to enable user defined profile power ramping of an external RF power transmitter stage.

The RAM contents are addressed incrementally by first setting bit 6 of RamDac Control register. While this bit is low, the RAM address pointer is held reset. The first two data words are written by writing to addresses $14 to $17 in order. Accessing location $17 post-increments the address pointer. Bit 7 of the RamDac Control register determines whether a read or write operation will increment the RAM address pointer. Further write operations to addresses $14 to $17, will load the next two locations.

All locations are accessed incrementally; further accesses to this port while bit 7 of the RamDac Control register is active are not valid and may cause data loss.

5.3.4 Aux ADC 0-5 Data Registers $08-13 Read

$08-09	Aux ADC 0	Auxiliary ADC 0 Data Register LSB - MSB
$0A-0B	Aux ADC 1	Auxiliary ADC 1 Data Register LSB - MSB
$0C-0D	Aux ADC 2	Auxiliary ADC 2 Data Register LSB - MSB
$0E-0F	Aux ADC 3	Auxiliary ADC 3 Data Register LSB - MSB
$10-11	Aux ADC 4	Auxiliary ADC 4 Data Register LSB - MSB
$12-13	Aux ADC 5	Auxiliary ADC 5 Data Register LSB - MSB

$08, $0A, $0C, $0E, $10, $12

Bit	7	6	5	4	3	2	1	0
	X	X	X	X	X	X	ADC Data [1:0]	

$09, $0B, $0D, $0F, $11, $13

Bit	7	6	5	4	3	2	1	0
	ADC Data [9:2]							

These registers enable the user to inspect the conversion value for each of the six auxiliary ADCs. There are two read registers per ADC, one to obtain the two least significant bits of the data, the other for the eight most significant bits. Reading these registers does not affect the ADC conversion cycle. Reading the MSB register directly reads the ADC output and simultaneously causes the two bits in the LSB register to be written to a holding register. This holding register is read when the LSB register is read. This mechanism is necessary to allow the user to read MSB and LSB data from the same ADC conversion cycle. If only the MSB register is read, the converter can be considered as an 8-bit ADC. If a 10-bit conversion is required, the MSB register must be read first.

5.3.5 Aux Control1 $11 Write

Bit:	7	6	5	4	3	2	1	0
	0	0	Enable ADC 5	Enable ADC 4	Enable ADC 3	Enable ADC 2	Enable ADC 1	Enable ADC 0

This register controls which ADC channels are converted. These bits may be changed at any time, but will only update the active state of the ADC channel for the next time it is converted.

5.3.6 Aux Control2 $12 Write

Bit:	7	6	5	4	3	2	1	0
	DAC RAM Polarity	Reset DAC RAMs	0	0	0	Conversion rate	Enable cont conversion	Start conversion

If bit 6 is set to '1' the RAM associated with DAC 0 is reset, if bit 7 is high the RAM is reset to all 1's, if bit 7 is low the RAM is reset to all 0's. This feature can be used to avoid programming every RAM location when short ramp profiles are required.

Bit 2 selects the conversion rate of the auxiliary ADC. If set low, the ADC will be clocked at MCLK/16, giving a conversion time of 176 MCLK periods per enabled channel. Setting this bit high halves the ADC clock rate and doubles the conversion time.

Setting bit 1 high will cause each enabled ADC channels to be converted continuously.

Setting bit 0 high will cause a single conversion of all enabled ADC channels. This bit is automatically set low when the ADC conversion has been completed. Note that this bit only has an effect when bit 1 is set low.

5.4 Synthesiser

Two integer-N synthesisers are provided, one as the main RF synthesiser (Main PLL), which provides the tuneable frequency to enable channel selection, and the other (Aux PLL) for the generation of lower frequency for mixing from IF to baseband. These two synthesisers are fully programmable, via the processor interface, to any frequency in the range 600 MHz to 2 GHz and 150 MHz to 250 MHz respectively.

Both the synthesised frequencies are internally divided down. The main RF frequency is divided by two for use in the offset loop in the transmitter and also for the image reject mixer in the receiver. Note that, in order to obtain quadrature signals for the IR mixer, both the rising and falling edges of the VCO generated signal are used; it is important, therefore, that the VCO produce a waveform that is as close as possible to a mark to space ratio of one. The second synthesiser is optionally divided by 2 or 4 for the transmitter and divided by 4 for the receiver.

Both synthesisers are phase locked loops (PLLs) and utilise external VCOs and loop filters. The phase noise of the VCOs should be adequate for the application with particular attention paid to the performance of the main VCO. It will be noted that as the CMX990 includes an internal divide-by-two in the LO path the PLL phase noise will be improved by approximately 6dB. The loop filters will need to be designed as required based on switching bandwidths, VCO gain etc. The CMX990 phase detectors are of the phase-frequency type with a high impedance charge pump output requiring just passive components in the loop filter. As a result standard design equations for a type II PLL can be used to select loop filter components. Lock detect functions are built in to each synthesiser and the status reported to the host processor. In particular, a transition to out-of-lock can be detected and communicated via an interrupt to the processor if required; this can be important to ensure that the transmitter cannot falsely transmit into other bands in the event of a fault condition arising.

The minimum step size is also programmable by setting the reference division ratio; to minimise the effects of phase noise this should be kept as high as possible, particularly on the main RF synthesiser. For Mobitex, the maximum this can be set to is 25 kHz as this is governed by the 12.5 kHz channel spacing and the subsequent divide-by-2 of the generated frequency. Note that if it is required to select a frequency that is 6.25 kHz offset from a convenient division of the main frequency (although still with 12.5 kHz channel spacings), it is better to keep the step size at 25 kHz but slightly offset the reference oscillator. In this way the phase noise and lock time performance will not be compromised.

Each synthesiser is set up using two registers, an ‘N’ register that sets the division value of the input reference frequency to the comparison frequency (step size), and an ‘M’ register that sets the division of the required synthesised frequency from the external VCO to the comparison frequency.

In the main PLL the VCO frequency is pre-scaled by 2 prior to being divided by N there therefore there is a factor of 2 in the formula that yields a required synthesised frequency (Fs) such that:

$$Fs = (2 \times N / M) \times F_{REF}$$ where F_{REF} is the reference oscillator frequency

For the aux PLL the formula is:

$$Fs = (N / M) \times F_{REF}$$

Main and Aux PLL

Input

The main and aux PLL circuits have control registers as listed below. Writing to the least significant 8 bits will trigger the circuit to update the dividers with the new multi byte value. Whenever the enable bit is low the divider circuit will be in the inactive 'zero power' (ZP) mode. To enter normal operation from ZP mode the MSB (including the enable bit) is written, the LSB would be written last, this would simultaneously enable the PLL and load the divider ratio - lock may take longer when exiting ZP mode. To enter ZP mode only the MSB need be written, double buffering will not be used for this control line - a simple SET / RESET latch will store the 'Enable' value, SET from the output of the 2nd buffer, RESET from the inverted output of the 1st buffer. The main and aux PLL will control their outputs to the required quiescent value when shutting down.

Output

One buffered digital output line from each PLL will indicate when the relevant PLL is in lock, this output is not synchronised. '1' = PLL enabled and in lock, '0' = all other conditions (including disabled ZP state). These lock outputs are terminated the status register in the host interface block and can optionally cause an external interrupt to occur. See section 5.2.3 for a description of interrupt operation.

Main PLL M divider $20-21 Write

Bit:	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	Main PLL Enable	Tx LO DIV	0	MSB					LSB							

The 'Tx LO DIV' bit controls a divide by 2 stage in the Tx LO clock path, '1' = divide by 1, '0' = divide by 2.

Main PLL N divider $22-23-24 Write

Bit:	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	Sign	0	0	0	MSB				NSB								LSB							

The 'Sign' bit controls the polarity of the Rx IF summer, a '0' = summation, '1' = subtraction.

Aux PLL M divider $25-26 Write

Bit:	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	Aux PLL Enable	Tx IF Filter		MSB					LSB							

The 'Tx IF Filter' bits control the Tx IF filter frequency:

Bit 6	Bit 5	Tx IF filter setting
0	0	90 MHz
0	1	80 MHz
1	0	45 MHz
1	1	40 MHz

Aux PLL N divider $27-28 Write

Bit:	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	Tx IF DIV	0	MSB						LSB							

The 'Tx IF DIV' bit controls a divide by 2 stage in the Tx IF clock path, '0' = divide by 1, '1' = divide by 2.

Sign, Tx IF DIV and Tx IF Filter control:

To activate the above control bits the required value must be written to the MSB register followed by a write to the LSB of the relevant divider.

5.5 RF and IF

This comprises the transmitter and receiver parts which, being half duplex, are only operated mutually exclusively. Normally the non-utilised part will be powered down when not in use. For single antenna operation an external transmit/receive (T/R) switch is required.

The CMX990 is designed as a broadband RF system. The RF section can support transmission and reception between 400MHz and 1GHz. As with any RF system care is required with frequency planning to minimise component count, avoid spurious responses etc. Examples of typical frequency planning are shown in section 5.5.2.

The transmitter takes the baseband I and Q signals from the modem and up-converts them via a quadrature modulator to a suitable Intermediate Frequency (IF). The summed output from this mixer will be an FM representation of the required transmit signal but at a lower frequency than that required. An offset PLL is then used to control an external VCO. The output of the VCO is sampled, usually after amplification, and mixed down to the IF value; this mixed down signal is then phase/frequency compared with the IF from the quadrature modulator. The output of the phase comparator is fed to an external loop filter, which controls the VCO thereby closing the loop. The VCO output then will be an FM signal at the required RF frequency having a low out-of-band spurious typical of VCO driven transmitters whilst guaranteeing a modulation index of exactly 0.5. The output of the VCO requires amplifying with an external PA (Power Amplifier).

The receiver requires use of an external LNA with some pre-filtering and an external balun. The differential output from the balun goes into an image reject down-mixer to a suitable IF (typically 45 MHz). The IF is filtered with an external filter to remove spurious signals and then goes into an AGC with a gain control range of 45dB. The output of the AGC is then mixed down to I and Q signals at baseband via a quadrature mixers. The I and Q signals are then amplified and filtered to remove any signals that may alias with the subsequent A-D sampling. The amplifier also has a coarse offset removal system to allow the approximate nulling of DC offsets developed in the circuits that may restrict the dynamic range in the subsequent processing.

5.5.1 Receiver Section

It is expected that the signal from the T/R switch will be amplified via an external LNA. The use and positioning of an image reject filtering is up to the radio designer. As a guide, the Mobitex specification requires a minimum of 45dB of first image rejection of which at least 25dB will be provided by the on-chip image reject mixer stage. The design is optimised with an LNA gain of about 15dB. It has been assumed that there is some insertion loss prior to the LNA; but an overall noise figure of 4dB and gain of 10dB (appox.) is achieved by the circuits preceding the CMX990. A digital control is available from the chip to enable/disable the LNA. A balun must be used to produce a reasonably well-balanced differential signal to the first mixer on the chip.

The Image Reject Mixer down-converts the signal to 45 MHz, although this frequency may be changed for use in regions where there may be conflicts with local transmissions. The resulting IF is then output from the chip as a single ended signal for filtering. It is expected that a relatively low cost crystal filter can be used to remove spurious signals some distance from the carrier. This is essential to meet the blocking performance required by the Mobitex specification. For detail filter requirements see Table 2.

The IF-signal from the filter is then taken back on chip to an AGC. This AGC is adjustable in steps of 15dB from -5dB to +40dB. This can be adjusted automatically, if enabled, by the chip or may be controlled by instruction from the host processor.

The output from the AGC is then mixed down to baseband, by a quadrature mixer stage, to produce I and Q signals. These are then filtered, to remove unwanted mixer products, spurii and remaining blocking signals and at the same time amplified to a suitable level for subsequent A-D conversion. The filters also precondition the signal to prevent aliasing with the A-D sample frequency. Channel filtering is provided digitally in the baseband processing section.

5.5.2 Transmitter Section

I and Q signals, which are baseband representations of the required FM signal, are up-converted with a quadrature modulator stage to a suitable value. The summed output from this stage has the required modulation index but at a lower frequency (TXIF) than that required for transmission.

An Offset Phase Locked Loop is used to translate this modulated frequency to the appropriate carrier frequency. The forward power signal is an attenuated version of the transmitted signal. This is taken on chip and further attenuated (if necessary) before being down-mixed with the main LO signal to a frequency nominally the same as the TXIF value. The resulting signal is taken off chip and low-pass filtered to remove unwanted mixer products, then passed back on to the chip. A high gain limiting amplifier is then used to enable the loop to have a high dynamic range and to lock-in even when the transmitted signal is very small and just starting to ramp up. The output of the limiting amplifier is then phase/frequency compared with the TXIF signal, the charge pump output being passed off chip into a suitable loop filter. The filtered output controls a VCO with its nominal frequency set to the middle of the required transmission band. Setting the loop filter appropriately allows the loop to follow the frequency modulations so as to give an exact modulation index of 0.5 whilst having the low spurii in transmission typical of a VCO based system.

The output of the VCO needs to be amplified appropriately with a Power Amplifier. A special feature of one of the Auxiliary D-A converters may be used to control the ramping of the power amplifier optimally should this be required. This feature is explained in the auxiliary section. The Auxiliary A-D section can also be used for sensing the forward and reverse power values, and the PA temperature should these features be required.

Rx band (MHz)		Tx band (MHz)		Rx IF	Rx Hi/	Rx LO (MHz)		Tx IF	IF Div	Tx LO (MHz)		LO Range
Bottom	Top	Bottom	Top	(MHz)	Lo bit	Bottom	Top	(MHz)	Setng	Bottom	Top	(MHz)
935	941	896	902	45	High	1960	1972	84	/2	1960	1972	12
864	870	819	825	45	High	1818	1830	90	/2	1818	1830	12
850	864	814	819	45	High	1790	1818	81-90	/2	1790	1818	28
426.6	429.5	416.6	419.5	45	Low	763.2	769	40	/4	753.2	759	15.8
423.9	426.6	413.9	416.6	45	Low	757.8	763.2	40	/4	747.8	753.2	15.4
440	440.6	425.5	426.1	45	Low	790	791.2	40	/4	771	772.2	20.2
450	453	460	463	45	High	990	996	40	/4	1000	1006	16
453.1	453.4	459.6	459.9	45	High	996.2	996.8	40	/4	999.2	999.8	3.6
415.7	418	406.2	408.5	45	Low	741.4	746	40	/4	732.4	737	13.6
421	423.9	411	413.9	45	Low	752	757.8	40	/4	742	747.8	15.8
419.5	420.5	412.5	413.5	45	Low	749	751	40	/4	745	747	6
427	427.5	419	419.5	45	Low	764	765	40	/4	758	759	7

Table 1 – Possible Frequency Plan for CMX990 in common Mobitex Frequency bands

5.5.3 Alternative Receiver Architecture

In circumstances where it is required to have a higher performance regarding intermodulation products (for instance to meet ETS 300 113) or to save some current that results from the use of an image reject mixer, it is possible to bypass the receiver front end completely and power these down. In this case the front end functions can be carried out using external components. The transmit mixer divide by two function should be disabled in this case and the VCO would operate at half the frequency.

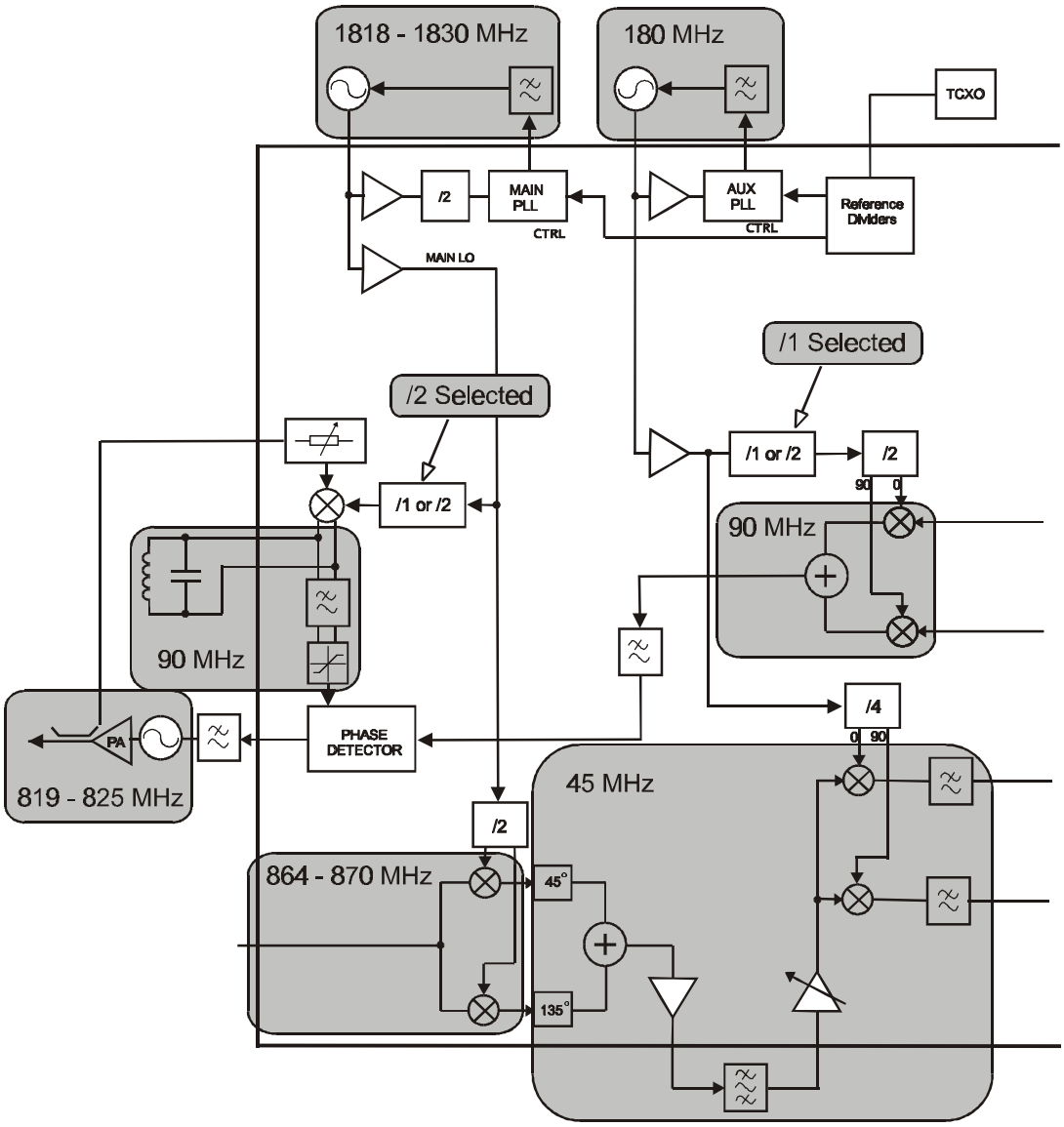


Figure 21 Simplified Block Diagram of CMX990 Showing Example Frequency Plan for 864-870MHz (Rx) / 819-825MHz (Tx) band

6. Application Notes

6.1 General

The CMX990 chip is a modem and RF system designed for wireless data modem applications. The chip addresses the needs of various data systems, both product standards and regulatory requirements, including:

- Mobitex Interface Standard (MIS)
- European R&TTE (based on EN 300 113)
- FCC Limits (47 CFR Parts 2 and 90)

Details of techniques to meet these requirements can be found in following sections.

6.2 Transmitter

The transmitter architecture is optimised for constant envelope phase/frequency modulation, typically GMSK or GFSK. The transmitter uses an offset phase locked loop (OPLL) to generate the transmitted signal. This has the advantage of very low spurious output minimising the need for spurious filtering reducing the overall cost of the radio and maximising power efficiency due to reduced losses.

The OPLL works by generating the modulation on an intermediate frequency (IF). This can be set on the CMX990 by programming the IF PLL to an appropriate IF. Table 1 shows some possible choices for these values and an example is shown in Figure 21. The CMX990 provides either divide by 2 or divide by 4 from the programmed local oscillator frequency to aid IF selection. The modulation is generated using classic I/Q vector modulation to provide an accurate modulated waveform which can also be inverted to allow high side or low side offset mixing (see section 5.1.4.4). This modulated signal is used as one input to a phase detector. The output of the phase detector drives a VCO operating directly on the desired transmitter frequency, via a suitable loop filter. The VCO output can be fed directly to power amplifier stages. The output of the PA is sampled, a directional coupler is recommended although a simple sample of the PA output can be used. This is fed to a mixer which translates the output frequency to the same IF as the reference modulation. The mixer output should be filtered to remove harmonics which could cause false locking and degrade vector error and is then fed back to the second input of the phase detector via a limiter. The limiter is used to ensure optimum signal level for the phase detector and to remove any AM content in the envelope although this should be negligible. The limiter has a wide input range, this is useful during loop start up as the loop will start locking with very small signals such that by the time output power rises towards operating levels the loop is already locked and the VCO on the correct frequency.

Output power can be controlled by the PA gain. This is typically done by applying a suitable ramp to the PA gate bias. This can be done either open loop or using a power detector and integrator to form a power levelling feedback loop. Details will depend on the PA device selected to work with the CMX990. The CMX990 provides a power ramping table on auxiliary DAC 1 to allow a suitable ramp profile to be applied. The auxiliary ADC can be used for a temperature sensor if software based ramping and output power compensation is used.

Start up

The timing of the turn-on of the transmitter needs careful control. Typical timings are shown in Figure 23. The first step is to program the IF and RF synthesisers to the correct frequencies for the desired transmitter channel. When time has been allowed for the PLL's to lock the transmitter circuits (excluding the PA) should be enabled. Depending on the leakage through the PA the OPLL should start to lock up. The limiter has been designed to start to lock with a signal 81dB below the maximum operating power. For a +35dBm transmitter this is -46dBm or 10dB below the common spurious emissions limit of -36dBm. The loop should lock quickly and power ramping can start before the loop is fully locked. If leakage

levels through the PA are particularly low it may be necessary to provide a small amount of bias to increase leakage to start locking.

Consider the following requirements from Mobitex MIS19:

- The receive to transmit time requirement is 20ms.
- Frequency must be within 200Hz of the final frequency before the start of data transmission.
- The carrier must “on” between 5ms and 10ms prior to the start of data.

The definition of carrier “on” is not very clear in the standard but if we assume 10ms is used for CPU processing and PLL locking, the transmitter power ramping could start at 10ms before data. The ramp could take 5ms to rise allowing a further 5ms for the frequency to obtain fine lock to within 200Hz. These times should be ample.

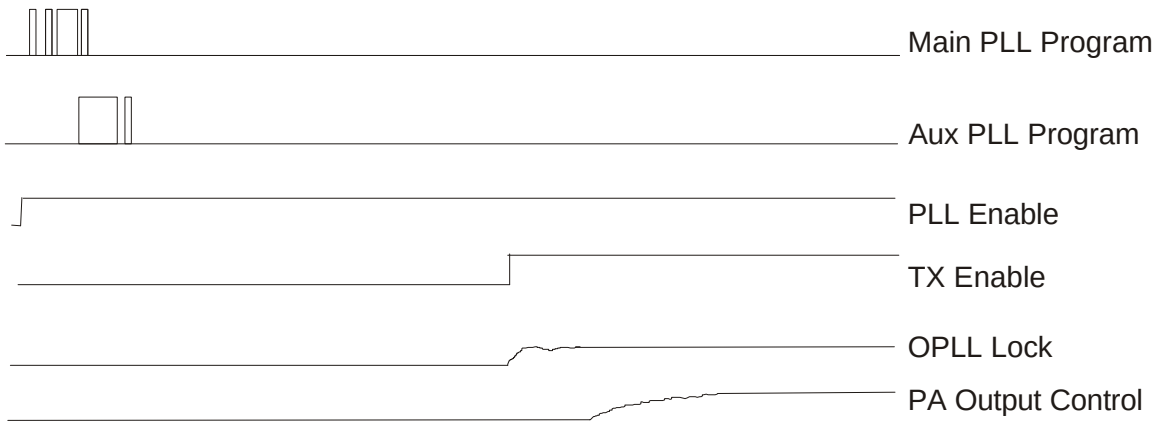


Figure 22 TX Timing Diagram (not to scale)

Spurious Emissions

The low level and small number of spurious emissions from the OPLL transmitter are a major advantage of the technique. The major source of spurious signals is the power amplifier harmonics. The level of these will be set by the selected PA and a harmonic filter must be provided to remove these. The only significant spurious signals generated by the OPLL transmitter is LO leakage from the offset mixer to the RF input port. The CMX990 mixer has been designed to have low local oscillator leakage meeting the typical requirements (e.g. -36dBm in Europe, -17dBm in USA).

Modulation Spectrum

The modulation of the CMX990 is produced digitally ensuring excellent accuracy and adjacent channel characteristics. The design meets EN 300 113 requirements in Europe and 47 CFR 2.1049 & 90.210 (J) applicable in the USA (Figure 23).

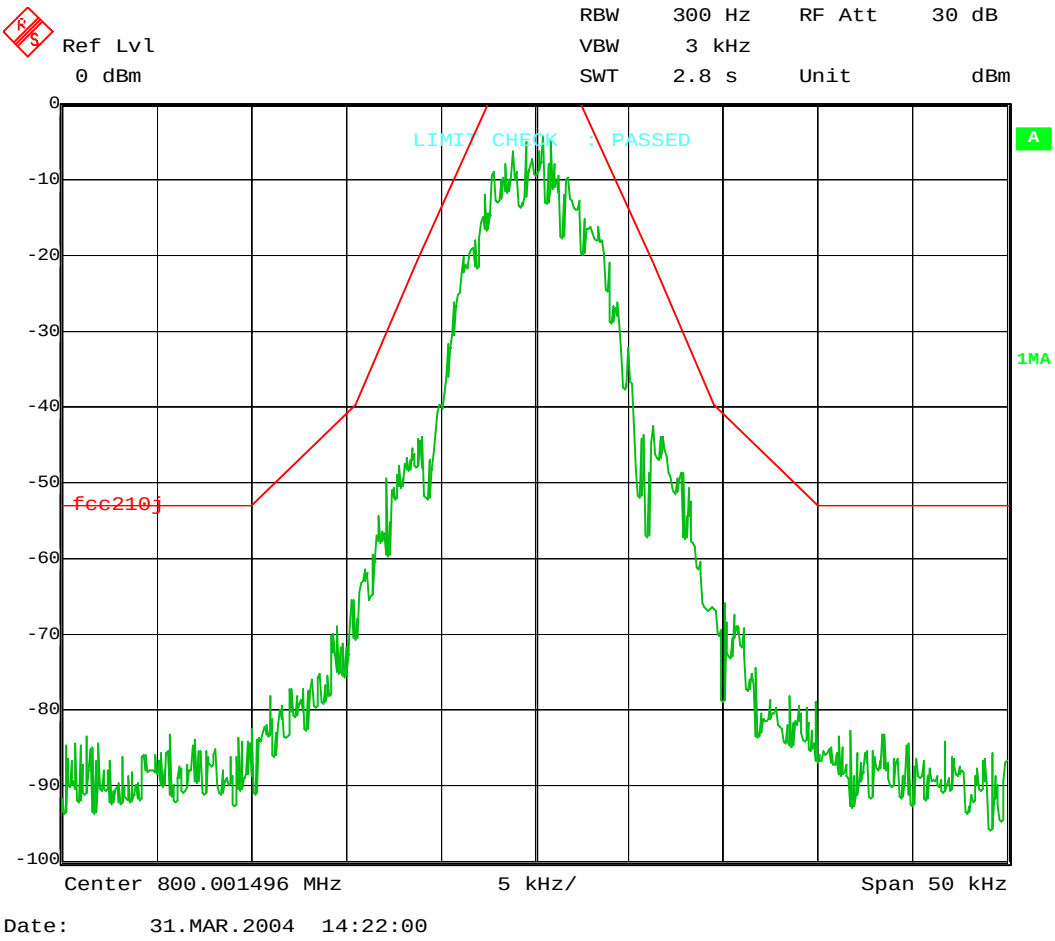


Figure 23 Modulation from CMX990 with 47 CFR 90.210 (J) emission mask

6.3 Receiver

The design of the CMX990 is such as to allow receiver requirements of the Mobitex standard to be met. In addition the receiver is also capable of meeting the requirement of standards such as EN 300 113 although in this case an external 1st mixer is required.

Architecture Overview

The receiver architecture is based on the classic superhetrodyne approach. The CMX990 provides the 1st mixer and IF stages with AGC followed by conversion to I/Q format baseband signals. These are then converted to digital signals in sigma-delta converters, which also provide adjacent channel filtering, before demodulation.

The first stage of the CMX990 receiver is a mixer intended to convert from RF to a 1st intermediate frequency (IF) of around 45MHz. The mixer is an image reject type thus minimising the external filters required before the mixer. The mixer would normally be preceded by input transmit/receive switch, low noise amplifier and a filter. A typical noise figure for these stages is around 4dB with a recommended gain of around 10dB. The noise figure of the mixers is very good for an image reject mixer (circa 13dB) minimising pre-gain required to achieve a reasonable overall noise figure. It will be noted that the mixer is a Gilbert cell type therefore requires a differential input. This can be achieved with a narrow-band LC circuit or a balun transformer. The image reject network is selectable to give high side or low side rejection depending on the frequency plan of RF and LO inputs.

The image reject 1st mixer has been optimised to provide a minimum cost solution. The CMX990 provides the option to bypass the 1st mixer to achieve a lower overall power consumption and/or better intermodulation performance using an external 1st mixer. Further details can be found below.

Following the 1st mixer the signal is passed off chip. A single ended output stage is used to ease connection to IF filter components. The 1st IF can be in the range 44-46MHz with 45MHz being a typical choice. Filtering is required at this point to achieve the Mobitex requirements and more stringent filtering to meet EN 300 113. For Mobitex adjacent channel filtering can be met with digital filters at baseband, however the blocking signal test at 84dB puts severe demands on the dynamic range of the baseband sections so filtering at the IF is necessary. A 2-pole crystal filter is recommended. EN 300 113 has more severe adjacent channel requirements so adjacent channel selectivity at the 1st IF is recommended. A 4-pole crystal filter should be satisfactory. A summary of filter requirements can be found in Table 2. A typical gain, noise figure and intermodulation partition is shown in Table 3 which assumes the filter performance specified in Table 2.

Frequency Offset	**Radio Modem Mode** (2 Pole Filter Recommended)	**EN 300 113 Mode** (4 Pole Filter Recommended)
12.5 kHz	10dB	30dB
25 kHz	15dB	30dB
50 kHz	25dB	50dB
100 kHz	25dB	50dB
1 MHz to 10 MHz	40dB	50dB
Pass band (≥ ±3.5 kHz)	3dB Typical	3dB Typical

Note: Attenuation relative to the pass band (with the exception of the pass band specification)

Table 2 IF Filter Requirements

					CMX990 Stages				
		Switch	LNA	BPF	1st Mixer	IF Filter	AGC/iq	Digital Filter	Output
Stage specifications:									
Gain	(dB)	-1.0	15.0	-3.5	-4.0[1]	-4.5	63.0	0.0	0.0
NF	(dB)	1.0	2.9	3.5	13.0	4.5	8.1	0.0	0.0
i/p IP	(dBm)	40.0	0.0	40.0	6.5	40.0	-44.0	99.0	99.0
i/p cp	(dBm)	30.0	-15.0	30.0	-2.0	30.0	-54.0	99.0	99.0
Cumulative response:									
preGain	(dB)	0.0	-1.0	14.0	10.5	6.5	3.5	66.5	66.5
Cum NF	(dB)	8.4	7.4	20.5	17.0	11.1	8.1	0.0	0.0
i/p Te	(%)	4.4	20.4	0.8	28.9	3.8	41.6	0.0	0.0
Cum IP	(dBm)	-13.1	-14.1	0.9	-2.6	-3.5	-44.0	97.5	99.0
i/p IM	(%)	0.0	0.2	0.0	75.9	0.0	24.0	0.0	0.0

Table 3 Typical Gain / Noise Figure / Intermodulation Partition for CMX990

The IF input stage goes into a gain controlled low noise amplifier stage. 45dB of AGC range is available in 15dB steps. The output of the IF amplifiers passes to I/Q mixers which are fed a by a divide by 4 circuit from the IF local oscillator. The mixers include DC offset compensation. Baseband amplifiers are then used to provide the correct input level to the ADC. The baseband amplifiers also include 55dB of rejection at the ADC image frequency of 1.92MHz. This combined with at least 40dB of external rejection from the IF filter provides adequate rejection to meet Mobitex requirements.

The ADC are sigma delta types providing high dynamic range and adjacent channel rejection. Internal DC offset correction is provided to maximise the useable range. After the ADC demodulation is provided

[1] Including loss of passive output matching

along with RSSI/AGC algorithms. RSSI is available from a register. AGC can be controlled automatically or manually. The baseband section also provides AFC measurement. Results are available to the host and can be used (via Aux DAC 1) to control an external reference oscillator.

DC Calibration

The signal levels in the receiver are small, typically only a few mV at sensitivity. For the demodulator algorithms to work correctly the DC offset must be reduced well below the level of the signal. To do this the CMX990 has two types of DC correction. Systematic DC offsets can be corrected by turning off the front end circuitry (Figure 24) and measuring the remaining signal then applying an appropriate correction. This process can be carried out automatically by the CMX990. An output control signal is provided from the chip to enable/disable the external LNA with appropriate timing. The result should correct the analogue signals prior to ADC stage to an error of less than 0.5mV. This maximises the dynamic range available from the ADC.

The second element of DC offset correction is based on averaging the received signal. This is done as part of the demodulator section and the correction applied by adding/subtracting the measured DC offset to the received data samples.

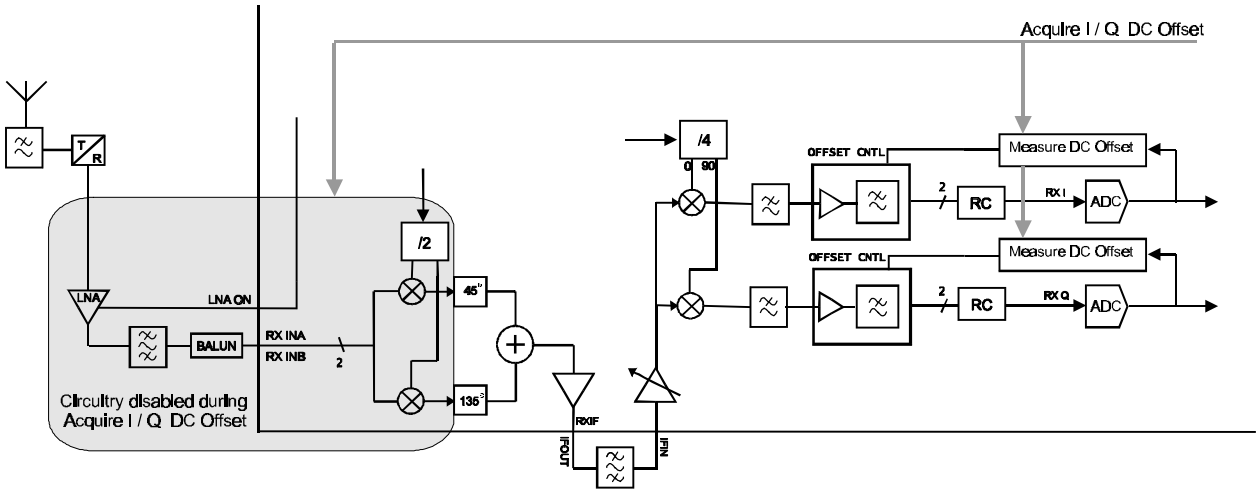


Figure 24 DC Offset Correction Scheme

Rx Mixer Options

The receive mixer in the CMX990 is a image reject type allowing a reduction in external filtering thus allowing a minimum cost solution. Certain radio modem products may require better intermodulation performance than can be achieved with the image reject architecture. In this case the an external mixer is recommended and to simplify external circuits the CMX990 incorporates a bypass switch for the transmit loop local oscillator divide-by-2. This allows the CMX990 transmit local oscillator to be re-used in an external mixer. A typical configuration is shown in figure 25.

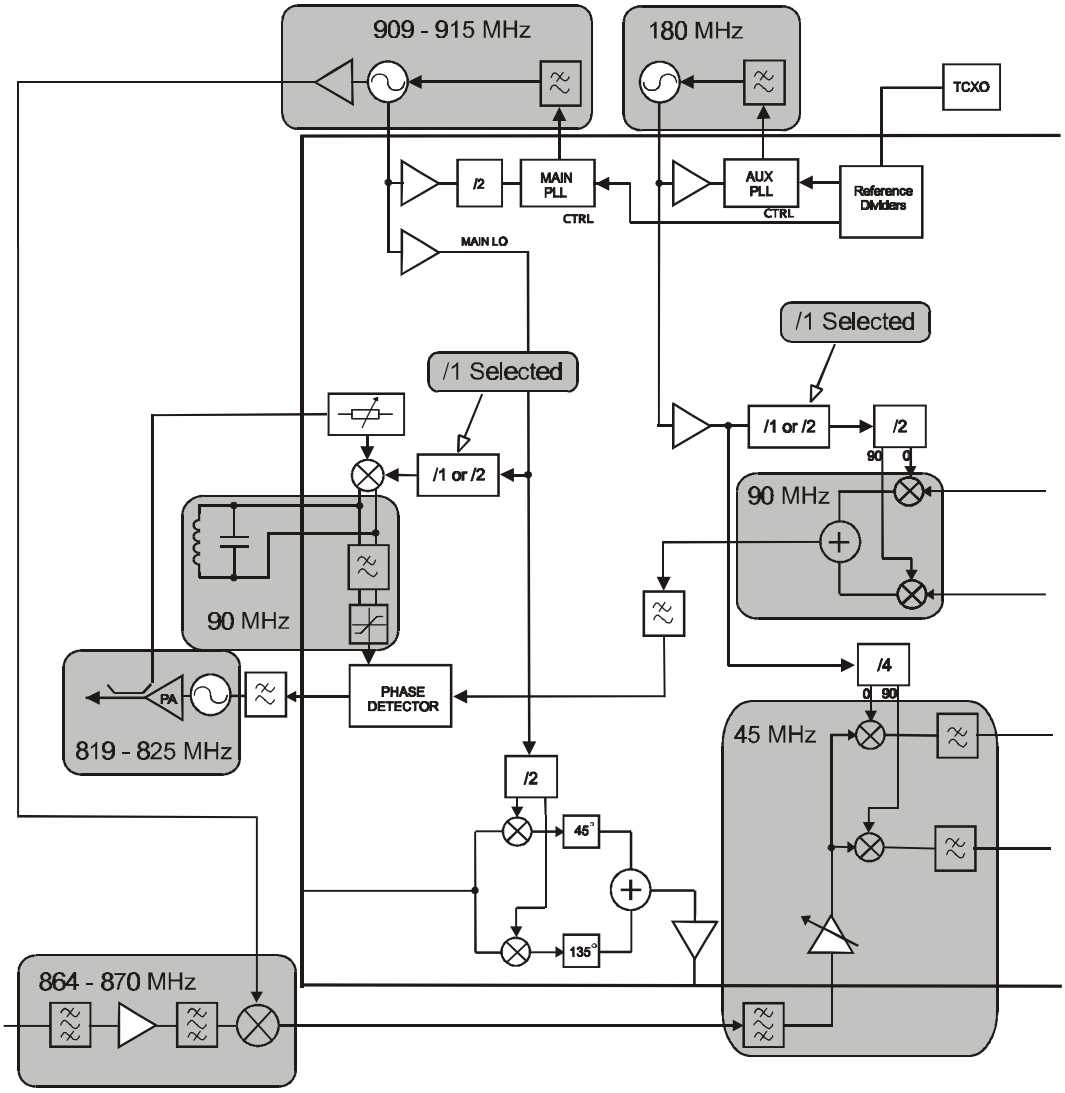


Figure 25 Block Diagram of CMX990 Showing use of External Receive Mixer

Signal to Noise

The performance of the receiver is based on the signal to noise performance of the demodulator. This has been shown to achieve the Mobitex error rate limit of 1 in 100 BER at 9dB C/N.

Dynamic Range, RSSI and AGC

The dynamic range of the receiver must be partitioned between various requirements. Key to this is the dynamic range of the ADC within IC that converts the I/Q signals into the digital domain. These converters have a dynamic range of at least 85dB. This must be partitioned between various factor such as filtering headroom, signal noise, quantisation noise margin etc. leaving an operating window. The proposed partition is shown in Figure 26. Other partitions are possible depending on adjacent channel requirements, external filtering, external gains etc.

The CMX990 has a built in AGC algorithm. Programmable gain has 4 steps of 15dB (i.e -5dB, +10dB, +25dB and +40dB). It is beneficial to allow as large an operating window as possible as the AGC has a certain amount of hysteresis allowing the signal to rise more than 15dB before the gain is backed off.

The CMX990 measures the signal level in baseband. This information is used to control the AGC but is also available via the control interface. This information must be combined with the AGC setting to determine RSSI.

Signal Processing

The CMX990 includes the demodulation functions, these are implemented digitally. Algorithms are consistent with Mobitex mobile burst timing structure and requirements. The received waveform can be inverted to allow high side or low side mixing in the receiver (see section 5.1.4.4). It will be noted that when powered on the CMX990 needs to acquire base channel. The baseband has been optimised to achieve this while also giving minimum power consumption in normal operation (i.e. maximum sleep times).

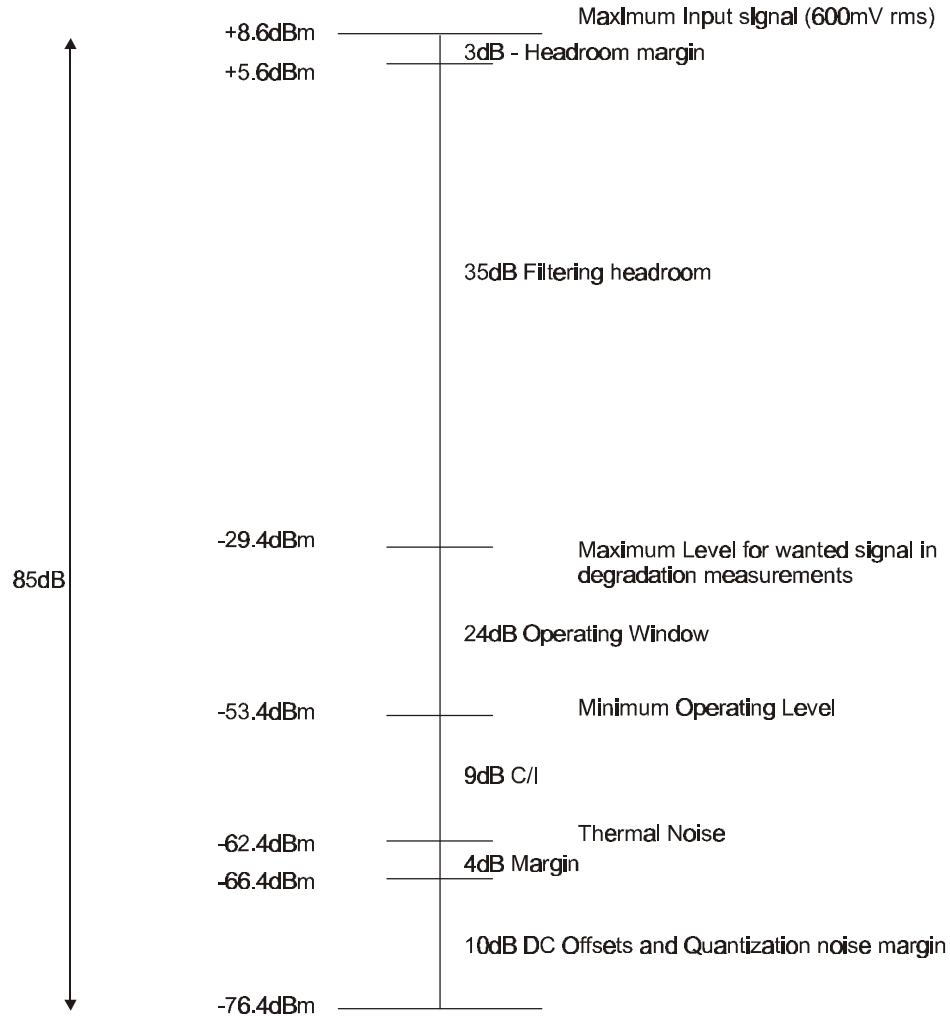
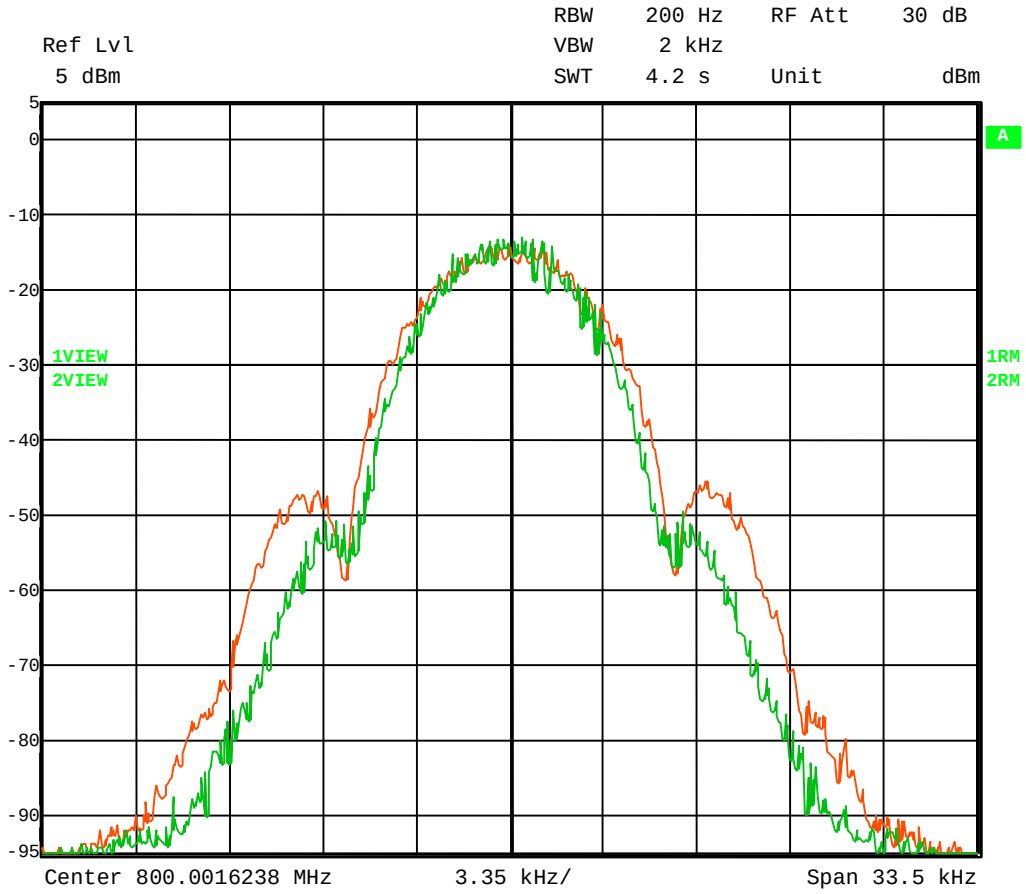


Figure 26 ADC Input Dynamic Range Partition

6.4 Variable B_t

The CMX990 offers the ability to select the B_t factor in the transmit modulation. This allows characteristics to be optimised for a particular bit/rate channel bandwidth. Standard options of B_t = 0.3 and B_t = 0.5 are available. Figure 27, 28 and 29 show the effect of changing B_t.



Inner Trace is CMX990 with B_t = 0.3 Outer Trace is CMX990 with B_t = 0.5

Figure 27 Modulation spectrum of CMX990 at 8kbps with different B_t

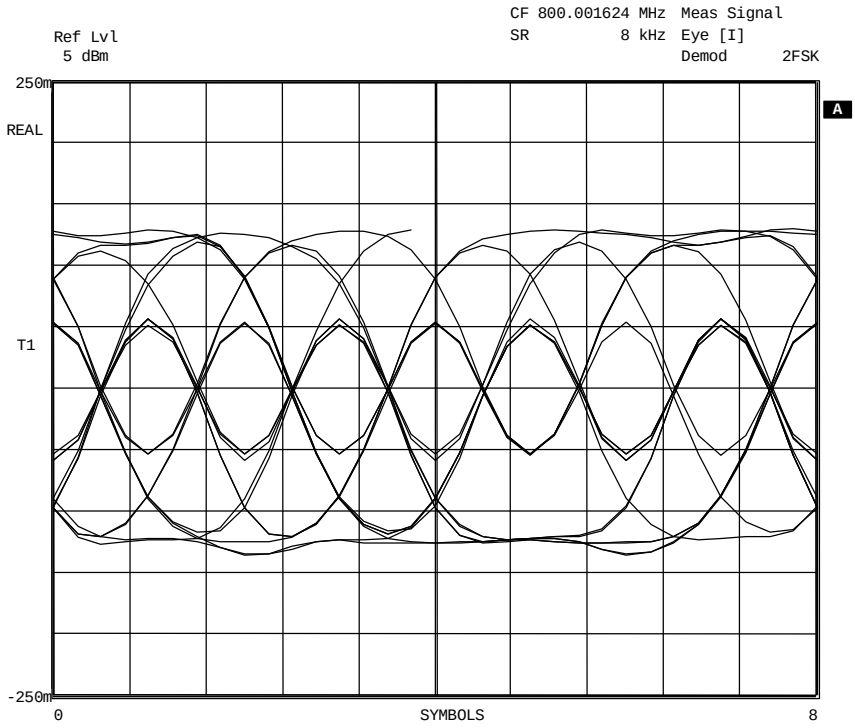


Figure 28 CMX990 modulation eye diagram at 8kbps with B_t = 0.3 (Measurement filter B_t=1)

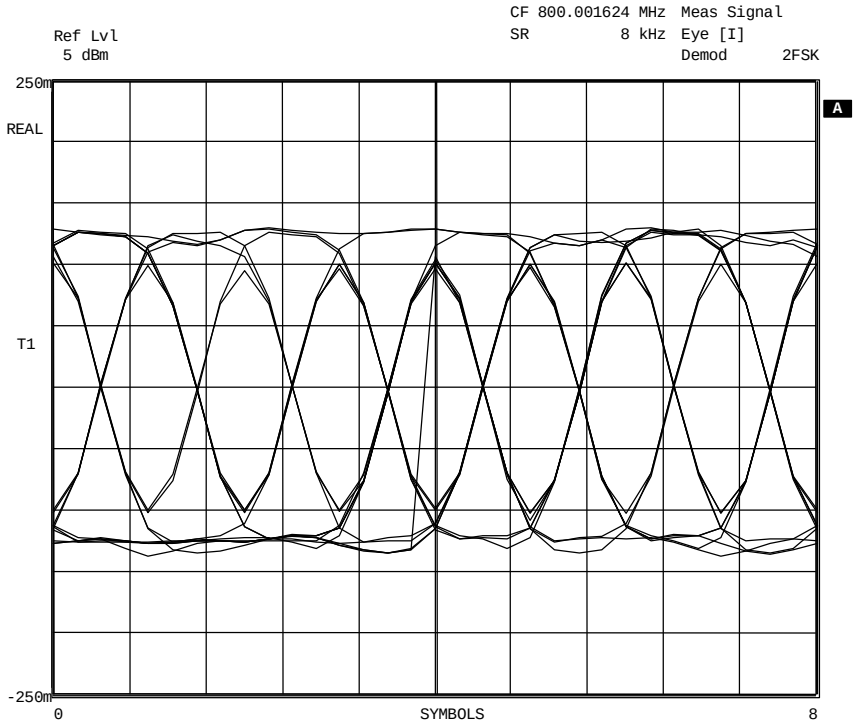


Figure 29 CMX990 modulation eye diagram at 8kbps with B_t = 0.5 (Measurement filter B_t=1)

7. Performance Specification

7.1 Electrical Performance

7.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Unit
Supply (V_{DDH} - V_{SSH} and V_{DDVCO} - V_{SSH} only)	-0.3	4.0	V
Supply (All other V_{DD} - V_{SS})	-0.3	3.0	V
Voltage on any pin to V_{SSH}	-0.3	V_{DD} + 0.3	V
Current into or out of any V_{DD} or V_{SS} pin	-100	+100	mA
Current into or out of any other pin	-20	+20	mA
Voltage between any 2 V_{SS} pins	-0.3	+0.3	V
Voltage between any 2 V_{DD} pins (except V_{DDH})	-0.3	+0.3	V

Q1 Package	Min.	Max.	Unit
Total Allowable Power Dissipation at T_{AMB} = 25 °C	–	1000	mW
... Derating above 70 °C	–	26.5	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

7.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (V_{DDH} - V_{SSH})		3.0	3.6	V
Supply (V_{DDVCO} - V_{SSH})		3.0	3.6	V
Supply (All other V_{DD} - V_{SSH})		2.25	2.75	V
Voltage difference between supplies:				
V_{DDH} to V_{DDVCO}		0	±0.2	V
Between all other V_{DD}		0	±0.2	V
All V_{SS} to V_{SSH}		0	±50	mV
Operating Temperature		-40	+85	°C
Clock Frequency	1	3.8	24	MHz

Notes: 1 Error in RF and IF frequencies and bit rate is directly related to the clock frequency.

7.1.3 Operating Characteristics

Details in this section represent design target values and are not currently guaranteed.

For the following conditions unless otherwise specified:

Clock Frequency = 19.2MHz, Bit Rate = 8k bits/sec, Noise Bandwidth = Bit Rate,
$V_{DDH} = V_{DDVCO}$ = 3.0V to 3.6V, T_{AMB} = -40°C to +85°C.

	Notes	Min.	Typ.	Max.	Unit
DC Parameters					
I_{DD} (powersaved) at V_{DDH} = 3.3 V	2	–	5.0	20	µA
Tx I_{DD} at V_{DDH} = 3.3 V	2	–	65	100	mA
Rx I_{DD} at V_{DDH} = 3.3 V	2	–	85	120	mA
AC Parameters					
Clock Input					
'High' pulse width	3	20	–	–	ns
'Low' pulse width	3	20	–	–	ns
Signal amplitude		0.5	–	–	V p-p
Input impedance (at 19.2 MHz)		TBD	–	–	Ω
µC Interface					
Input logic "1" level	4, 5	80%	–	–	V_{DDH}
Input logic "0" level	4, 5	–	–	20%	V_{DDH}
Input leakage current (Vin = 0 to V_{DDH})	4, 5	-5.0	–	+5.0	µA
Input capacitance	4, 5	–	10	–	pF
Output logic "1" level (I_{OH} = 120 µA)	5	90%	–	–	V_{DDH}
Output logic "0" level (I_{OL} = 360 µA)	5, 6	–	–	10%	V_{DDH}
'Off' state leakage current (Vout = V_{DDH})	6	–	–	10	µA

	Notes	Min.	Typ.	Max.	Unit
AC Parameters					
Rx 1st Mixer					
Input frequency range		400	–	950	MHz
Local oscillator frequency range	8	700	–	2000	MHz
IF output frequency		44	45	46	MHz
Gain	7	–	0.5	–	dB
Input third order intercept point		TBD	+13	–	dBm
Image rejection		TBD	30	–	dB
Input impedance		–	TBD	–	Ω
Output load		–	600	–	Ω
Output noise voltage		–	4.9	–	nV/√Hz
Rx IF Stages					
Input frequency range		44	45	46	MHz
Input third order intercept (Max Gain)		–	TBD	–	dBm
Input impedance		–	650	–	Ω
Noise figure		–	8	–	dB
Maximum gain (Max AGC)		–	63	–	dB
Minimum gain (Min AGC)		–	18	–	dB
AGC step size		–	15	–	dB
AGC step size accuracy		–	±1.5	–	dB
Selectivity at ±1 to 10 MHz		10	–	–	dB
Selectivity at ±1.92 MHz (ADC Alias)		55	–	–	dB
I/Q image rejection		TBD	30	–	dB
Local oscillator range	13	176	180	184	MHz
RSSI output			Digital		
Tx Offset Mixer					
Input frequency range		400	–	950	MHz
Local oscillator frequency range	8	700	–	2000	MHz
IF output frequency		40	–	90	MHz
Input level		TBD	–	TBD	dBm
Conversion gain		–	TBD	–	dB
Tx Limiter/Modulator/Phase Detector					
Input frequency range		40	–	90	MHz
Combined rms phase error		–	3.8	–	deg
Combined peak phase error		–	14	–	deg
Charge pump output current		–	±1.0	–	mA
Normal input level	9	-35	–	-10	dBm
Total limiting range	9	-91	–	-10	dBm
Input Impedance			high		Ω
IF input frequency	12	160	–	180	MHz

	Notes	Min.	Typ.	Max.	Unit
Auxiliary ADC					
Resolution		–	10	–	bits
Input range	14	TBD	–	TBD	V
Auxiliary DAC	15				
Resolution		–	10	–	bits
Output range		TBD	–	TBD	V
Phase Locked Loop					
Reference Input					
Frequency		TBD	19.2	TBD	MHz
Level	10	0.5	–	–	Vp-p
Divide ratios	11	1	–	8192	
Main RF Synthesizer					
Comparison frequency		–	–	500	kHz
Input frequency range		600	–	2000	MHz
Input level		-10	–	-20	dBm
Divide ratios		48000	–	1048576	
Charge pump current		–	±2.5	–	mA
Normalised SSB phase noise		–	152	–	dBc/Hz
Aux IF Synthesizer					
Comparison frequency		–	100	600	kHz
Input frequency range		150	–	250	MHz
Input level		-10	–	-20	dBm
Divide ratios		250	–	16384	
Charge pump current		–	±2.5	–	mA
Normalised SSB phase noise		–	TBD	–	dBc/Hz

Notes:

2. Not including any current drawn from the device pins by external circuitry.
3. Timing for the external input to the CLOCK pin.
4. WRN, RDN, CSN, A0 - A5 pins.
5. D0 - D7 pins.
6. IRQN pin.
7. Gain shown is for a matched 50Ω source, however the input is high impedance and a transformer or equivalent voltage step-up circuits can be used to achieve a higher gain figure. If such arrangements are used input third order intercept point will be degraded.
8. A divide by 2 is provided within the IC.
9. Normal input level is the range over which phase error performance is specified. The total limiting range is an extended range, the lower end of which is intended to allow the Tx loop to “lock up” during power up.
10. Sine wave or clipped sine wave.
11. Separate dividers provided for RF and IF PLL’s
12. TX LO chain has selectable divide by 2 or divide by 4.
13. IC contains divide by 4.
14. Aux ADC 2 and 3 have uncommitted op-amps on the input.
15. Aux DAC 0 provides a power ramp for the PA passed on a user-programmable ramp table. Aux DAC 1 should be connected to VCXO (or VCTCXO) for AFC control.

7.1.3 Operating Characteristics (continued)

Timing Diagrams

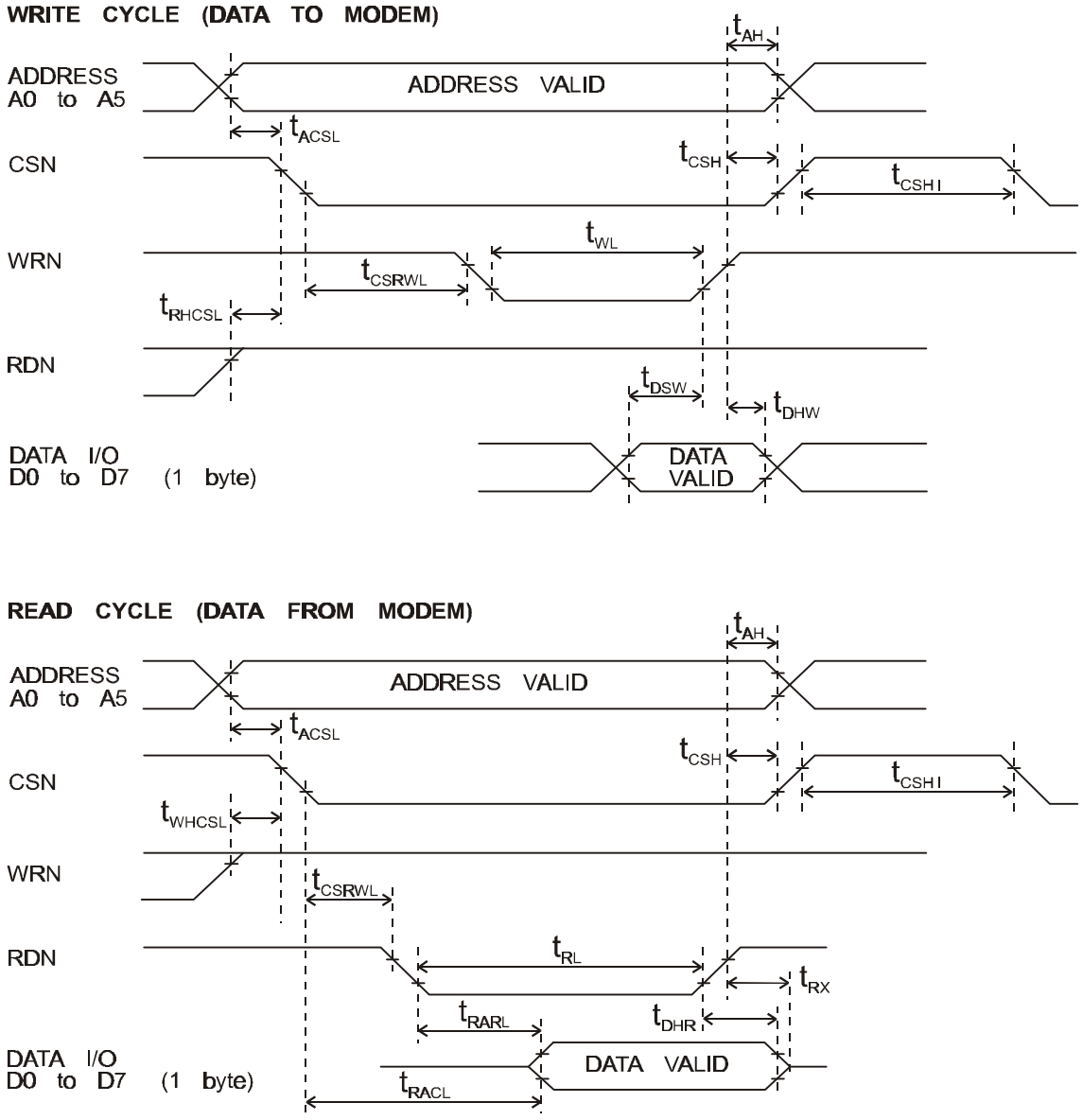


Figure 30 µC Parallel Interface Timings

For the following conditions unless otherwise specified:

Clock Frequency = 19.2MHz, V_{DDH} = 3.0V to 3.6V, T_{AMB} = -40°C to +85°C.

		Notes	Min.	Typ.	Max.	Unit
Parallel Interface Timings (ref. Figure 24)					–	
t_{ACSL}	Address valid to CSN low time		0	–	–	ns
t_{AH}	Address hold time		10	–	–	ns
t_{CSH}	CSN hold time		0	–	–	ns
t_{CSHI}	CSN high time		6	–	–	clock cycles
t_{CSRWL}	CSN to WRN or RDN low time		0	–	–	ns
t_{DHR}	Read data hold time		0	–	–	ns
t_{DHW}	Write data hold time		0	–	–	ns
t_{DSW}	Write data setup time		90	–	–	ns
t_{RHCSL}	RDN high to CSN low time (write)		0	–	–	ns
t_{RACL}	Read access time from CSN low	18	–	–	175	ns
t_{RARL}	Read access time from RDN low	18	–	–	145	ns
t_{RL}	RDN low time		200	–	–	ns
t_{RX}	RDN high to D0-D7 3-state time		–	–	50	ns
t_{WHCSL}	WRN high to CSN low time (read)		0	–	–	ns
t_{WL}	WRN low time		200	–	–	ns

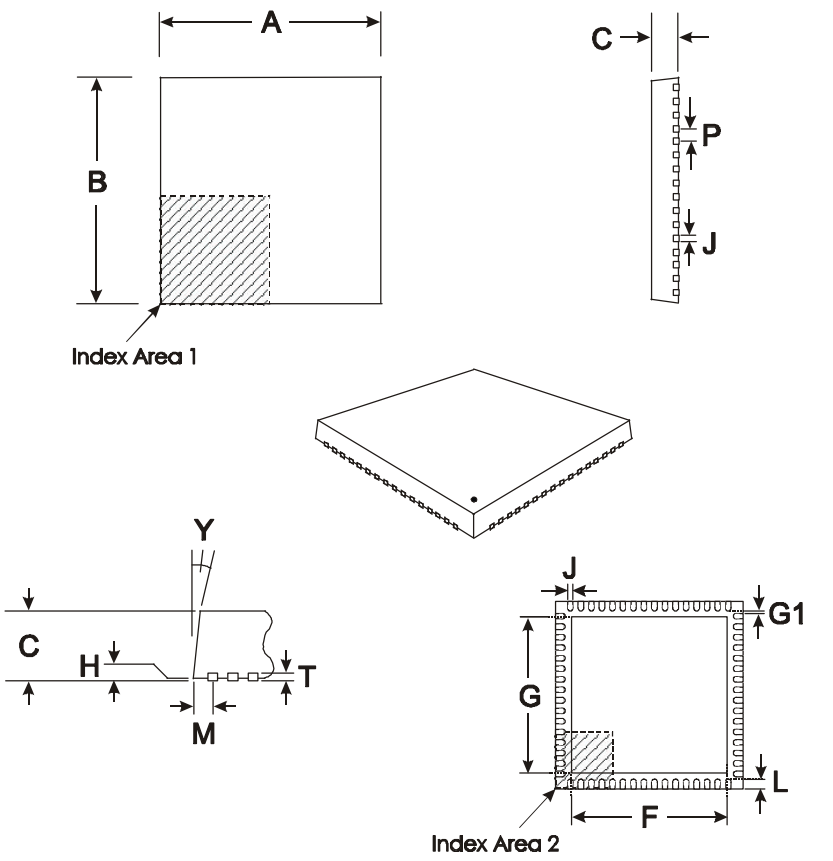
Notes:

18. With 30pF max to V_{SS} on D0 - D7 pins. Data valid at greater of: t_{RARL} + t_{CSRWL} or t_{RACL}.

TBD

Figure 31 Typical Bit Error Rate

7.2 Packaging



	DIM.	MIN.	TYP.	MAX.
*	A	8.80		9.20
*	B	8.80		9.20
	C	0.80		1.00
	F	7.00		7.95
	G	7.00		7.95
	G1		0.225	
	H	0.00		0.05
	J	0.18		0.30
	L	0.30		0.50
	M		0.75	
	P		0.50	
	T		0.20	
	Y	0°		12°

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees

Index Area 1 Index Area 2

Note:

The underside of the Q1 package is conductive and should be electrically connected to the analogue ground. The circuit board should be designed so that no unwanted short circuits can occur.

Figure 32 Q1 Mechanical Outline: *Order as part no. CMX990Q1*

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